SCLD001

High-speed CMOS Logic Data Book

1983

Silicon-gate Complementary MOS

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GENERAL INFORMATION 1

RATINGS AND CHARACTERISTICS 2

DESCRIPTIVE INFORMATION 3

EXPLANATION OF LOGIC SYMBOLS 4

ORDERING INSTRUCTIONS AND MECHANICAL DATA 5

IC SOCKETS 6

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1983

Texas Instruments is pleased to announce the SN74HC family of high-speed CMOS logic circuits. This versatile new family promises to be the product family of choice for many new logic systems, offering a unique combination of high-speed, low-power dissipation, high noise immunity, wide fanout capability, extended supply voltage range, and high reliability.

This data book describes the initial product line scheduled for introduction during 1983. Included are pinout and package information, logic symbols, maximum ratings and dc electrical characteristics. At the time of this edition, JEDEC recommendations for ac performance have not been finalized, consequently the timing requirements and switching characteristics for each device have been left blank. However, as each new family member is released, TI will publish the corresponding ac parameters, which may be obtained from your nearest TI field sales office or your local authorized TI distributor. Later editions of this data book will contain complete ac specifications.

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1

GENERAL INFORMATION

Alphanumeric Index 1-2

Glossary 1-4

Functional Index/Selection Guide 1-7

Explanation of Function Tables 1-12

Parameter Measurement Information 1-14

ALPHANUMERIC INDEX

TYPE NUMBERS	RATINGS AND CHARACTERISTICS* TABLE	RATINGS AND CHARACTERISTICS* PAGE	DESCRIPTIVE INFORMATION† PAGE	TYPE NUMBERS	RATINGS AND CHARACTERISTICS* TABLE	RATINGS AND CHARACTERISTICS* PAGE	DESCRIPTIVE INFORMATION PAGE
'HC00	I	2-3	3-2	'HC173	III	2-5	3-80
'HC02	I	2-3	3-3	'HC174	IV	2-6	3-82
'HC04	I	2-3	3-4	'HC175	II	2-4	3-82
'HC08	I	2-3	3-5	'HC189	III	2-5	3-84
'HC10	I	2-3	3-6	'HC190	IV	2-6	3-87
'HC11	I	2-3	3-7	'HC191	IV	2-6	3-87
'HC14	I	2-3	3-8	'HC192	IV	2-6	3-91
'HC20	I	2-3	3-9	'HC193	IV	2-6	3-91
'HC21	I	2-3	3-10	'HC194	IV	2-6	3-95
'HC27	I	2-3	3-11	'HC195	IV	2-6	3-98
'HC30	I	2-3	3-12	'HC221	IV	2-6	3-100
'HC32	I	2-3	3-13	'HC240	III	2-5	3-102
'HC36	I	2-3	3-14	'HC241	III	2-5	3-102
'HC42	IV	2-6	3-15	'HC242	III	2-5	3-104
'HC51	I	2-3	3-17	'HC243	III	2-5	3-104
'HC73	II	2-4	3-18	'HC244	III	2-5	3-106
'HC74	II	2-4	3-20	'HC245	III	2-5	3-108
'HC75	II	2-4	3-22	'HC251	III	2-5	3-110
'HC76	II	2-4	3-24	'HC253	III	2-5	3-112
'HC77	II	2-4	3-26	'HC257	III	2-5	3-114
'HC78	II	2-4	3-28	'HC258	III	2-5	3-114
'HC85	IV	2-6	3-30	'HC259	IV	2-6	3-116
'HC86	I	2-3	3-32	'HC266	I	2-3	3-118
'HC107	II	2-4	3-34	'HC273	IV	2-6	3-119
'HC109	II	2-4	3-36	'HC280	IV	2-6	3-121
'HC112	II	2-4	3-38	'HC299	III	2-5	3-123
'HC113	II	2-4	3-40	'HC323	III	2-5	3-126
'HC114	II	2-4	3-42	'HC352	III	2-5	3-129
'HC123	IV	2-6	3-44	'HC353	III	2-5	3-131
'HC132	I	2-3	3-46	'HC354	III	2-5	3-133
'HC133	I	2-3	3-47	'HC356	III	2-5	3-136
'HC137	IV	2-6	3-48	'HC365	III	2-5	3-139
'HC138	IV	2-6	3-50	'HC366	III	2-5	3-139
'HC139	IV	2-6	3-52	'HC367	III	2-5	3-139
'HC147	IV	2-6	3-54	'HC368	III	2-5	3-139
'HC151	III	2-5	3-56	'HC373	III	2-5	3-141
'HC152	III	2-5	3-58	'HC374	III	2-5	3-143
'HC153	III	2-5	3-60	'HC377	IV	2-6	3-145
'HC154	IV	2-6	3-62	'HC378	IV	2-6	3-145
'HC157	III	2-5	3-64	'HC379	II	2-4	3-145
'HC158	III	2-5	3-64	'HC386	I	2-3	3-148
'HC160	IV	2-6	3-66	'HC390	IV	2-6	3-149
'HC161	IV	2-6	3-66	'HC393	IV	2-6	3-149
'HC162	IV	2-6	3-66	'HC423	IV	2-6	3-152
'HC163	IV	2-6	3-66	'HC490	IV	2-6	3-154
'HC164	IV	2-6	3-72	'HC533	III	2-5	3-156
'HC165	IV	2-6	3-74	'HC534	III	2-5	3-158
'HC166	IV	2-6	3-77	'HC563	III	2-5	3-160

*See these pages for absolute maximum ratings, recommended operating conditions, and electrical characteristics.

†See these pages for description, pin assignments, timing requirements, and switching characteristics.

TEXAS INSTRUMENTS
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TYPE NUMBERS	RATINGS AND CHARACTERISTICS* TABLE	RATINGS AND CHARACTERISTICS* PAGE	DESCRIPTIVE INFORMATION† PAGE
'HC564	III	2-5	3-162
'HC573	III	2-5	3-164
'HC574	III	2-5	3-166
'HC590	III	2-5	3-168
'HC592	IV	2-6	3-170
'HC593	III	2-5	3-170
'HC594	III	2-5	3-173
'HC595	III	2-5	3-175
'HC597	IV	2-6	3-177
'HC598	III	2-5	3-177
'HC620	III	2-5	3-180
'HC623	III	2-5	3-180
'HC640	III	2-5	3-183
'HC643	III	2-5	3-183
'HC645	III	2-5	3-183
'HC646	III	2-5	3-186
'HC648	III	2-5	3-186
'HC651	III	2-5	3-190
'HC652	III	2-5	3-190
'HC688	IV	2-6	3-194
'HC4002	I	2-3	3-196
'HC4017	IV	2-6	3-197
'HC4020	IV	2-6	3-199
'HC4040	IV	2-6	3-201
'HC4060	IV	2-6	3-203
'HC4075	I	2-3	3-205
'HC4078	I	2-3	3-206
'HC4511	IV	2-6	3-207
'HC4514	IV	2-6	3-209
'HC4515	IV	2-6	3-209
'HC4538	IV	2-6	3-212
'HC4724	IV	2-6	3-214

*See these pages for absolute maximum ratings, recommended operating conditions, and electrical characteristics.

†See these pages for description, pin assignments, timing requirements, and switching characteristics.

GLOSSARY
SYMBOLS, TERMS, AND DEFINITIONS

INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

OPERATING CONDITIONS AND CHARACTERISTICS (IN SEQUENCE BY LETTER SYMBOLS)

C_{pd} **Power dissipation capacitance**
Used to determine the no-load dynamic power dissipation per logic function (See individual circuit pages):
$P_D = C_{pd} V_{CC}^2 f + I_{CC} V_{CC}$.

f_{max} Maximum clock frequency
The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

I_{CC} **Supply current**
The current into* the V_{CC} supply terminal of an integrated circuit.

I_{IH} **High-level input current**
The current into* an input when a high-level voltage is applied to that input.

I_{IL} ***Low-level input current***
The current into* an input when a low-level voltage is applied to that input.

I_{OH} **High-level output current**
The current into* an output with input conditions applied that, according to the product specification, will establish a high level at the output.

I_{OL} **Low-level output current**
The current into* an output with input conditions applied that, according to the product specification, will establish a low level at the output.

I_{OS} **Short-circuit output current**
The current into* an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

I_{OZ} **Off-state (high-impedance-state) output current (of a three-state output)**
The current flowing into* an output having three-state capability with input conditions established that, according to the production specification, will establish the high-impedance state at the output.

V_{IH} **High-level input voltage**
An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.
NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

* Current out of a terminal is given as a negative value.

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V_{IL} **Low-level input voltage**
An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.
NOTE: A minimum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{OH} **High-level output voltage**
The voltage at an output terminal with input conditions applied that, according to product specification, will establish a high level at the output.

V_{OL} **Low-level output voltage**
The voltage at an output terminal with input conditions applied that, according to product specification, will establish a low level at the output.

V_{T+} **Positive-going threshold level**
The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{T-}.

V_{T-} **Negative-going threshold level**
The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{T+}.

t_a **Access time**
The time interval between the application of a specified input pulse and the availability of valid signals at an output.

t_{dis} **Disable time (of a three-state output)**
The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state. (t_{dis} = t_{PHZ} or t_{PLZ}).

t_{en} ***Enable time (of a three-state output)***
The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low). (t_{en} = t_{PZH} or t_{PZL}).

t_h **Hold time**
The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.
NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.

t_{pd} **Propagation delay time**
The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level. (t_{pd} = t_{PHL} or t_{PLH}).

t_{PHL} **Propagation delay time, high-to-low level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

t_{PHZ} **Disable time (of a three-state output) from high level**
The time interval between the specified reference points on the input and the output voltage waveforms with the three-state output changing from the defined high level to a high-impedance (off) state.

t_{PLH} **Propagation delay time, low-to-high-level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

t_{PLZ} **Disable time (of a three-state output) from low level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined low level to a high-impedance (off) state.

t_{PZH} **Enable time (of a three-state output) to high level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high level.

t_{PZL} **Enable time (of a three-state output) to low level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined low level.

t_{sr} **Sense recovery time**
The time interval needed to switch a memory from a write mode to a read mode and to obtain valid data signals at the output.

t_{su} **Setup time**
The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.

NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

t_w **Pulse duration (width)**
The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

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INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

FUNCTIONS	PAGE
AND/NAND Gates and Inverters	1-8
OR/NOR/EXCLUSIVE-OR and A-O-I Gates	1-8
Schmitt-trigger NAND Gates and Inverters	1-8
Bus Drivers and Transceivers with 3-State Outputs	1-8
Dual J-K Flip-flops	1-9
D-Type Flip-flops	1-9
Latches and Registers	1-9
Monostable Multivibrators	1-9
Shift Registers	1-10
Asynchronous Counters	1-10
Synchronous Counters	1-10
Comparators, Parity Generators/Checkers, and Priority Encoders	1-10
Data Selectors/Multiplexers	1-11
Decoders/Demultiplexers	1-11
Display Decoders/Drivers	1-11
Random-Access Memories (RAM's)	1-11

FUNCTIONAL INDEX/SELECTION GUIDE

AND, NAND GATES AND INVERTERS

(for Maximum Ratings and Electrical Characteristics See Table I, Page 2-3)

DESCRIPTION	DEVICE TYPE	DESCRIPTIVE INFORMATION
Hex Inverters	'HC04	3-4
Quad 2-Input NAND Gates	'HC00	3-2
Quad 2-Input AND Gates	'HC08	3-5
Triple 3-Input NAND Gates	'HC10	3-6
Triple 3-Input AND Gates	'HC11	3-7
Dual 4-Input NAND Gates	'HC20	3-9
Dual 4-Input AND Gates	'HC21	3-10
8-Input NAND Gate	'HC30	3-12
13-Input NAND Gate	'HC133	3-47

SCHMITT-TRIGGER GATES AND INVERTERS

(for Maximum Ratings and Electrical Characteristics See Table I, Page 2-3)

DESCRIPTION	DEVICE TYPE	DESCRIPTIVE INFORMATION
Hex Inverters	'HC14	3-8
Quad 2-Input NAND Gates	'HC132	3-46

OR, NOR, EXCLUSIVE-OR, AND AND-OR-INVERT GATES

(for Maximum Ratings and Electrical Characteristics See Table I, Page 2-3)

DESCRIPTION	DEVICE TYPE	DESCRIPTIVE INFORMATION
Quad 2-Input NOR Gates	'HC02	3-3
	'HC36	3-14
Quad 2-Input OR Gates	'HC32	3-13
Quad 2-Input EXCLUSIVE-NOR Gates	'HC266	3-118
Quad 2-Input EXCLUSIVE-OR Gates	'HC86	3-32
	'HC386	3-148
Dual 2-Wide 2-Input A-O-I Gates	'HC51	3-17
Triple 3-Input NOR Gates	'HC27	3-11
Triple 3-Input OR Gates	'HC4075	3-205
Dual 4-Input NOR Gates	'HC4002	3-196
8-Input NOR Gate	'HC4078	3-206

BUS DRIVERS AND TRANSCEIVERS WITH 3-STATE OUTPUTS

(for Maximum Ratings and Electrical Characteristics See Table III, Page 2-5)

DESCRIPTION	OUTPUT DATA	CONTROL INPUTS	DEVICE TYPE	DESCRIPTIVE INFORMATION
Quad Bus Transceivers	Inverting	Independent Enables for A and B Buses	'HC242	3-104
	True		'HC243	
Hex Bus Drivers/Receivers	True	Common Enables	'HC365	3-139
	Inverting		'HC366	
	True	Symmetrical Enables	'HC367	
	Inverting		'HC368	
Octal Bus Drivers/Receivers	Inverting	Symmetrical Enables	'HC240	3-102
	True	Complementary Enables	'HC241	
		Symmetrical Enables	'HC244	3-106
Octal Bus Transceivers	Inverting	Independent Enables for A and B Buses	'HC620	3-180
	True		'HC623	
	Inverting	Enable and Direction Control	'HC640	3-183
	True and Inverting		'HC643	
	True		'HC645	
			'HC245	3-108
Octal Bus Transceivers with Registers	True	Enable and Direction Control	'HC646	3-186
	Inverting		'HC648	
	Inverting	Independent Enables for A and B Buses	'HC651	3-190
	True		'HC652	

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D-TYPE FLIP-FLOPS

DESCRIPTION	OUTPUT CONFIGUATION	OTHER FEATURES	DEVICE TYPE	RATINGS AND CHARACTERISTICS TABLE	RATINGS AND CHARACTERISTICS PAGE	DESCRIPTIVE INFORMATION
Dual D-type Flip-flops with Preset and Clear	Complementary	Independent Clocks	'HC74	II	2-4	3-20
Quad D-Type Flip-flops with Common Clocks	Complementary	Common Clear	'HC175	II	2-4	3-82
		Output Enable	'HC379	II	2-4	3-145
Hex D-Type Flip-flops with Common Clocks	Q only	Common Clear	'HC174	IV	2-6	3-82
		Output Enable	'HC378	IV	2-6	3-145
Octal D-type Flip-flops with Common Clocks	Q only	Common Clear	'HC273	IV	2-6	3-119
		Output Enable	'HC377	IV	2-6	3-145
	3-State, Q only	Output Control	'HC374	III	2-5	3-143
			'HC574	III	2-5	3-166
	3-State, $\overline{Q}$ only	Output Control	'HC534	III	2-5	3-158
			'HC564	III	2-5	3-162

DUAL J-K FLIP-FLOPS

(for Maximum Ratings and Electrical Characteristics See Table II, Page 2-4)

DESCRIPTION	DEVICE TYPE	DESCRIPTIVE INFORMATION
Dual J-K Flip-flops with Clear	'HC73	3-18
	'HC107	3-34
Dual J-K Flip-flops with Preset	'HC113	3-40
Dual J-K Flip-flops with Preset, Common Clock, and Common Clear	'HC78	3-28
	'HC114	3-42
Dual J-K Flip-flops with Preset and Clear	'HC76	3-24
	'HC112	3-38
Dual J-$\overline{K}$ Flip-flops with Preset and Clear	'HC109	3-36

LATCHES AND REGISTERS

DESCRIPTION	OUTPUTS	DEVICE TYPE	RATINGS AND CHARACTERISTICS TABLE	RATINGS AND CHARACTERISTICS PAGE	DESCRIPTIVE INFORMATION
Quad D-type Latches	Complementary	'HC75	II	2-4	3-22
	Q only	'HC77	II	2-4	3-26
Quad D-type Registers	Q only, 3-state	'HC173	III	2-5	3-80
Octal D-Type Latches	Q only, 3-state	'HC373	III	2-5	3-141
		'HC573	III	2-5	3-164
	$\overline{Q}$ only, 3-state	'HC533	III	2-5	3-156
		'HC563	III	2-5	3-160
8-Bit Addressable Latches	Q only	'HC4724	IV	2-6	3-214
		'HC259	IV	2-6	3-116

MONOSTABLE MULTIVIBRATORS

(for Maximum Ratings and Electrical Characteristics See Table IV, Page 2-4)

DESCRIPTION	FEATURES		DEVICE TYPE	DESCRIPTIVE INFORMATION
Dual Monostable Multivibrators with Direct Clear, Postive and Negative Inputs, and complementary Outputs			'HC221	3-100
	Retriggerable		'HC123	3-44
		Will not trigger from clear	'HC423	3-152
			'HC4538	3-212

SHIFT REGISTERS

DESCRIPTION	INPUTS	OUTPUTS	DEVICE TYPE	RATINGS AND CHARACTERISTIC		DESCRIPTIVE INFORMATION
				TABLE	PAGE	
4-Bit Shift Register with Clear	J-$\overline{K}$/Parallel	Parallel	'HC195	IV	2-6	3-98
4-Bit Bidirectional Shift Registers with Clear	Serial/Parallel	Parallel	'HC194			3-95
8-Bit Shift Registers	Serial/Parallel, Clock Inhibit, Shift/Load	2 Serial	'HC165			3-74
	2 Serial, Clear	Parallel	'HC164			3-72
	Serial/Parallel, Clear, Clock Inhibit, Shift/Load	Serial	'HC166			3-77
8-Bit Shift Registers with Input Registers	Serial/Parallel	Serial	'HC597			3-177
	Serial/Parallel	3-state Parallel (Multiplexed I/O)	'HC598	III	2-5	3-177
8-Bit Bidirectional Shift Registers with Storage and Multiplexed 3-State I/O	Serial/Parallel	3-state Parallel	'HC299			3-123
			'HC323			3-126
8-Bit Shift Registers with Output Registers	Serial	Parallel	'HC594			3-173
		3-State Parallel	'HC595			3-175

SYNCHRONOUS COUNTERS

DESCRIPTION	FEATURES		TYPE	RATINGS AND CHARACTERISTICS		DESCRIPTIVE INFORMATION
				TABLE	PAGE	
Decade	Async Clear	Sync Load	'HC160	IV	2-6	3-66
	Sync Clear		'HC162			3-66
Decade Up/Down	Clock Inhibit	Async Load	'HC190			3-87
	Async Clear		'HC192			3-91
Divide-by-10 Johnson Counter	Async Clear		'HC4017			3-197
4-Bit Binary	Async Clear	Sync Load	'HC161			3-66
	Sync Clear		'HC163			3-66
4-Bit Binary Up/Down	Clock Inhibit	Async Load	'HC191			3-87
	Async Clear		'HC193			3-91
8-Bit Binary with Input Registers	Sync Clear		'HC592			3-170
		Multiplexed 3-state I/O	'HC593	III	2-5	3-170
8-Bit Binary with Output Registers	Sync Clear	3-state Outputs	'HC590			3-168

ASYNCHRONOUS (RIPPLE CLOCK) COUNTERS

(for Maximum Ratings and Electrical Characteristics See Table IV, Page 2-6)

DESCRIPTION	FEATURES	DEVICE TYPE	DESCRIPTIVE INFORMATION
12-Bit Binary Counters		'HC4040	3-201
14-Bit Binary Counters		'HC4020	3-199
	On-chip Oscillator	'HC4060	3-203
Dual Decade Counters	Bi-quinary or BCD	'HC390	3-149
	Set-to-9 Input	'HC490	3-154
Dual 4-Bit Binary Counters		'HC393	3-149

COMPARATORS, PARITY GENERATORS/ CHECKERS, AND PRIORITY ENCODERS

(for Maximum Ratings and Electrical Characteristics See Table IV, Page 2-6)

DESCRIPTION	DEVICE TYPE	DESCRIPTIVE INFORMATION
4-Bit Magnitude Comparators	'HC85	3-30
8-Bit Magnitude Comparators	'HC688	3-194
9-Bit Odd/Even Parity Generator/Checker	'HC280	3-121
10-Line Decimal to 4-Line BCD Priority Encoder	'HC147	3-54

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DATA SELECTORS/MULTIPLEXERS

(for Maximum Ratings and Electrical Characteristics See Table III, Page 2-5)

DESCRIPTION	INPUTS	OUTPUTS	DEVICE TYPE	DESCRIPTIVE INFORMATION
8-Line-to-1-Line		Inverting	'HC152	3-58
	Enable	Complementary	'HC151	3-56
		Complementary, 3-state	'HC251	3-110
	Transparent Latches, Enable	Complementary 3-state	'HC354	3-133
	Registers, Enable		'HC356	3-136
Dual 4-line-to-1-Line	Independent Enables	True, 3-state	'HC253	3-112
		Inverting, 3-state	'HC353	3-131
		True	'HC153	3-60
		Inverting	'HC352	3-129
Quad 2-Line-to-1-Line	Common Enable	True	'HC157	3-64
		Inverting	'HC158	3-64
		True, 3-state	'HC257	3-114
		Inverting, 3-state	'HC258	3-114

DECODERS/DEMULTIPLEXERS

(for Maximum Ratings and Electrical Characteristics See Table IV, Page 2-6)

DESCRIPTION	FEATURES	DEVICE TYPE	DESCRIPTIVE INFORMATION
4-Line-to-16-Line	2 Enables	'HC154	3-62
	Input latches, Output Enable	'HC4514	3-209
		'HC4515	3-209
4-Line-to-10-Line, BCD-to-Decimal		'HC42	3-15
3-Line-to-8-Line	3 Enables	'HC138	3-50
	3 Enables, Address Latches	'HC137	3-48
Dual 2-Line-to-4-Line	Independent Enables	'HC139	3-52

DISPLAY DECODERS/DRIVERS

DESCRIPTION	DEVICE TYPE	RATINGS AND CHARACTERISTICS		DESCRIPTIVE INFORMATION
		TABLE	PAGE	
BCD-to-7-Segment Decoders/Drivers with Input Latches	'HC4511	IV	2-6	3-207

RANDOM ACCESS MEMORIES

DESCRIPTION	ORGANIZATION	FEATURES	DEVICE TYPE	RATINGS AND CHARACTERISTICS		DESCRIPTIVE INFORMATION
				TABLE	PAGE	
64-Bit	16 x 4	3-state Outputs	'HC189	III	2-5	3-84

EXPLANATION OF FUNCTION TABLES

The following symbols are now being used in function tables on TI data sheets:

- H = high level (steady state)
- L = low level (steady state)
- ↑ = transition from low to high level
- ↓ = transition from high to low level
- X = irrelevant (any input, including transitions)
- Z = off (high-impedance) state of a 3-state output
- a . . h = the level of steady-state inputs at inputs A through H respectively
- Q_0 = level of Q before the indicated steady-state input conditions were established
- $\bar{Q}_0$ = complement of Q_0 or level of $\bar{Q}$ before the indicated steady-state input conditions were established
- Q_n = level of Q before the most recent active transition indicated by ↑ or ↓
-  = one high-level pulse
-  = one low-level pulse
- TOGGLE = each output changes to the complement of its previous level on each active transition indicated by ↑ or ↓.

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains, H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0, or $\bar{Q}_0$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse, or , the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

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Among the most complex function tables in this book are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. Below is the function table of a 4-bit bidirectional universal shift register, e.g., type SN74HC194.

FUNCTION TABLE

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	*a*	*b*	*c*	*d*	*a*	*b*	*c*	*d*
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{D0}

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

The second line shows that so long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Since on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs will occur while the clock remains high or on the high-to-low transition of the clock.

The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high then, without regard to the serial input, the data entered at A will be at output Q_A, data entered at B will be at Q_B, and so forth, following a low-to-high clock transition.

The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at Q_A is now at Q_B, the previous levels of Q_B and Q_C are now at Q_C and Q_D respectively, and the data previously at Q_D is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high and the levels at inputs A through D have no effect.

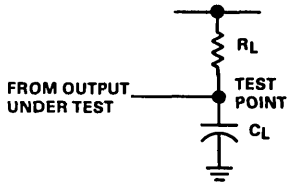
The sixth and seventh lines represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at Q_B is now at Q_A, the previous levels of Q_C and Q_D are now at Q_B and Q_C, respectively, and the data previously at Q_A is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

The last line shows that as long as both mode inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

PARAMETER MEASUREMENT INFORMATION

1

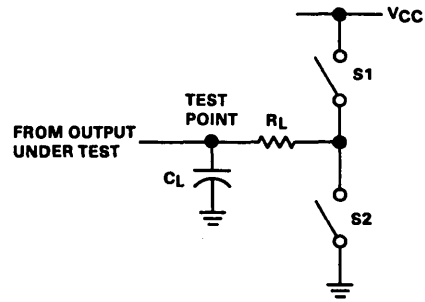
TOTEM POLE OUTPUTS



PARAMETER		R_L‡	C_L†‡
t_{PLH} or	Standard outputs	∞	50 pF
t_{PHL}	High-current outputs §	∞	150 pF

†C_L includes probe and test fixture capacitance.
‡These values apply only when alternative values (R_L = 2 kΩ, C_L = 15 pF) are not specified in the column heading in switching characteristics.
§High-current outputs are indicated by the ▷ in the logic symbol.

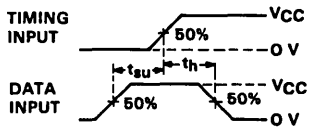
3-STATE OUTPUTS



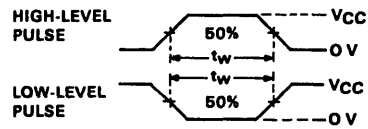
LOAD CIRCUIT

PARAMETER	R_L‡	C_L†‡	S_1	S_2
t_{PZH}	1 kΩ	5 pF	OPEN	CLOSED
t_{PZL}			CLOSED	OPEN
t_{PHZ}	1 kΩ	50 pF	OPEN	CLOSED
t_{PLZ}			CLOSED	OPEN
t_{PLH} or t_{PHL}	∞	75 pF	CLOSED	OPEN

†C_L includes probe and test fixture capacitance.
‡These values apply only when alternative values (R_L = 667Ω, C_L = 45 pF) are not specified in the column heading in switching characteristics.



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES*



VOLTAGE WAVEFORMS
PULSE WIDTHS*

* In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{out} ≈ 50Ω, t_r = 6 ns, t_f = 6 ns.

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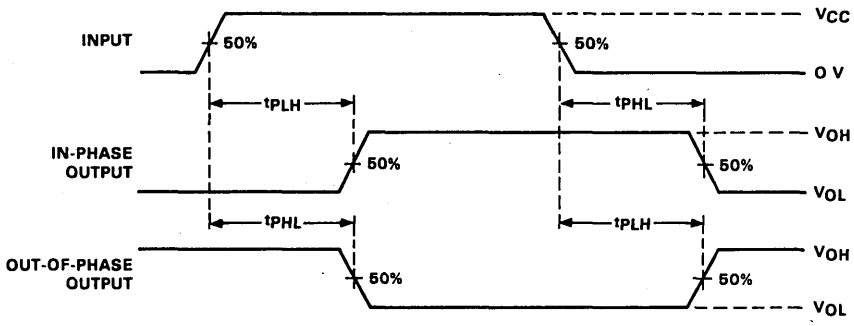
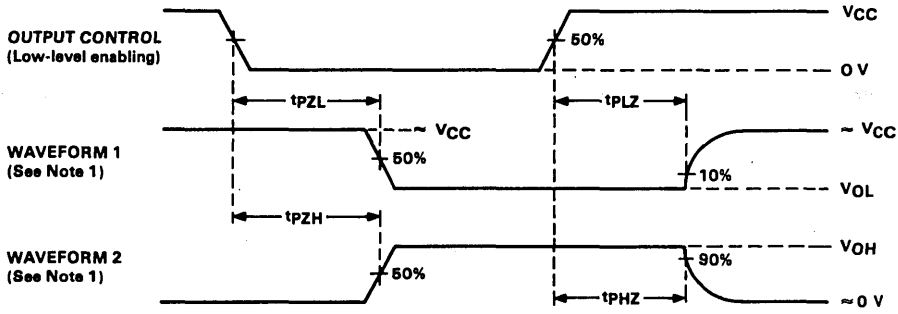


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES*



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS*

Note: 1. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

* In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.

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Ratings and Characteristics

2

ATTENTION

These devices contain circuits to protect the inputs and outputs against damage due to high static voltages or electrostatic fields; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits.

Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

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TABLE I
SPECIFICATIONS FOR SSI CIRCUITS

D2684, DECEMBER 1982

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... −0.5 to 7 V
Input diode current, I_{IK}($V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
Output diode current, I_{OK}($V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±20 mA
Continuous output current ($-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$) ..... ±25 mA
Continuous current through V_{CC} or GND pins ..... ±50 mA
Lead temperature 1,6 mm (1/16 in) from case: J package for 60 seconds ..... 300°C
N package for 10 seconds ..... 260°C
Storage temperature range ..... −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC'			SN74HC'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		2	5	6	2	5	6	V
V_{IH} High-level input voltage	V_{CC} = 4.5 V	3.15			3.15			V
	V_{CC} = 5 V	3.50			3.50			
	V_{CC} = 5.5 V	3.85			3.85			
V_{IL} Low-level input voltage	V_{CC} = 4.5 V	0		0.9	0		0.9	V
	V_{CC} = 5 V	0		1.0	0		1.0	
	V_{CC} = 5.5 V	0		1.1	0		1.1	
V_I Input voltage		−0.5		V_{CC} + 0.5	−0.5		V_{CC} + 0.5	V
V_O Output voltage		−0.5		V_{CC} + 0.5	−0.5		V_{CC} + 0.5	V
I_{OH} High-level output current				−4			−4	mA
I_{OL} Low-level output current				3.4			4	mA
t_t Input transition (rise and fall) times (except Schmitt-trigger inputs)		0		500	0		500	ns
T_A Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics, V_{CC} = 5 V ± 10%, over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54HC'		SN74HC'		UNIT
			MIN	TYP‡	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, V_{CC} = 4.5 V, I_{OH} = −4mA		3.86			3.56		3.70		V
	V_I = V_{IH} or V_{IL}, I_{OH} = −200 μA		V_{CC} −0.2	V_{CC}		V_{CC} −0.2		V_{CC} −0.2		
	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA		V_{CC} −0.1	V_{CC}		V_{CC} −0.1		V_{CC} −0.1		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 3.4 mA			0.27		0.4			V
		I_{OL} = 4 mA			0.32				0.4	
	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA			0	0.1		0.1		0.1	
$V_{T+} - V_{T-}$¶			0.4	1		0.4		0.4		V
I_I	V_I = V_{CC} or 0 V				±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or 0 V, I_O = 0				2		40		20	μA
C_i				3	10		10		10	pF

‡All typical values are at V_{CC} = 5 V.
¶This parameter applies only to Schmitt-trigger inputs.

switching characteristics

See individual circuit pages.

TABLE II
SPECIFICATIONS FOR DUAL AND QUAD FLIP-FLOPS AND LATCHES

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... −0.5 to 7 V
Input diode current, I_{IK} ($V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
Output diode current, I_{OK} ($V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±20 mA
Continuous output current ($-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$) ..... ±25 mA
Continuous current through V_{CC} or GND pins ..... ±50 mA
Lead temperature 1,6 mm (1/16 in) from case: J package for 60 seconds ..... 300°C
N package for 10 seconds ..... 260°C
Storage temperature range ..... −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC'			SN74HC'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		2	5	6	2	5	6	V
V_{IH} High-level input voltage	V_{CC} = 4.5 V	3.15			3.15			V
	V_{CC} = 5 V	3.50			3.50			
	V_{CC} = 5.5 V	3.85			3.85			
V_{IL} Low-level input voltage	V_{CC} = 4.5 V	0		0.9	0		0.9	V
	V_{CC} = 5 V	0		1.0	0		1.0	
	V_{CC} = 5.5 V	0		1.1	0		1.1	
V_I Input voltage		−0.5		V_{CC} + 0.5	−0.5		V_{CC} + 0.5	V
V_O Output voltage		−0.5		V_{CC} + 0.5	−0.5		V_{CC} + 0.5	V
I_{OH} High-level output current				−4			−4	mA
I_{OL} Low-level output current				3.4			4	mA
t_t Input transition (rise and fall) times		0		500	0		500	ns
T_A Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics, V_{CC} = 5 V ± 10%, over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54HC'		SN74HC'		UNIT
			MIN	TYP‡	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}, V_{CC} = 4.5 V, I_{OH} = −4mA		3.86			3.56		3.70		V
	$V_I = V_{IH}$ or V_{IL}, I_{OH} = −200 μA		V_{CC} −0.2	V_{CC}		V_{CC} −0.2		V_{CC} −0.2		
	$V_I = V_{IH}$ or V_{IL}, I_{OH} = −20 μA		V_{CC} −0.1	V_{CC}		V_{CC} −0.1		V_{CC} −0.1		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 3.4 mA			0.27		0.4			V
		I_{OL} = 4 mA			0.32				0.4	
	$V_I = V_{IH}$ or V_{IL}, I_{OL} = 20 μA			0	0.1		0.1		0.1	
I_I	$V_I = V_{CC}$ or 0 V				±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or 0 V, I_O = 0				4		80		40	μA
C_i				3	10		10		10	pF

‡All typical values are at V_{CC} = 5 V.

switching characteristics

See individual circuit pages.

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TABLE III
SPECIFICATIONS FOR CIRCUITS WITH HIGH-CURRENT OUTPUTS

D2684, DECEMBER 1982

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... −0.5 to 7 V
Input diode current, I_{IK}($V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
Output diode current, I_{OK}($V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±20 mA
Continuous output current (-0.5 V $< V_O < V_{CC} + 0.5$ V) ..... ±25 mA
Continuous current through V_{CC} or GND pins ..... ±50 mA
Lead temperature 1,6 mm (1/16 in) from case: J package for 60 seconds ..... 300°C
N package for 10 seconds ..... 260°C
Storage temperature range ..... −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC'			SN74HC'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		2	5	6	2	5	6	V
V_{IH} High-level input voltage	V_{CC} = 4.5 V	3.15			3.15			V
	V_{CC} = 5 V	3.50			3.50			
	V_{CC} = 5.5 V	3.85			3.85			
V_{IL} Low-level input voltage	V_{CC} = 4.5 V	0		0.9	0		0.9	V
	V_{CC} = 5 V	0		1.0	0		1.0	
	V_{CC} = 5.5 V	0		1.1	0		1.1	
V_I Input voltage		−0.5		V_{CC} + 0.5	−0.5		V_{CC} + 0.5	V
V_O Output voltage		−0.5		V_{CC} + 0.5	−0.5		V_{CC} + 0.5	V
I_{OH} High-level output current	High-current outputs ¶			−6			−6	mA
	Standard outputs			−3.4			−4	
I_{OL} Low-level output current	High-current outputs ¶			5.1			6	mA
	Standard outputs			3.4			4	
t_t Input transition (rise and fall) times		0		500	0		500	ns
T_A Operating free-air temperature		−55		125	−40		85	°C

¶High-current outputs are indicated by the ▷ in the logic symbol. All 3-state outputs are high-current outputs.

electrical characteristics, V_{CC} = 5 V ± 10%, over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54HC'		SN74HC'		UNIT
			MIN	TYP‡	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}, V_{CC} = 4.5 V, $I_{OH} = -4$mA		3.86			3.56		3.70		V
	$V_I = V_{IH}$ or V_{IL}, $I_{OH} = -200$ μA		V_{CC} −0.2	V_{CC}		V_{CC} −0.2		V_{CC} −0.2		
	$V_I = V_{IH}$ or V_{IL}, $I_{OH} = -20$ μA		V_{CC} −0.1	V_{CC}		V_{CC} −0.1		V_{CC} −0.1		
V_{OL}	$V_I = V_{IH}$ or V_{IL}, I_{OL} = max rec.	54HC'			0.27		0.4			V
		74HC'			0.32				0.4	
	$V_I = V_{IH}$ or V_{IL}, I_{OL} = 20 μA			0	0.1		0.1		0.1	
I_{OZ}§	$V_O = V_{CC}$ or 0 V, $V_I = V_{IH}$ or V_{IL}				±0.5		±5		±5	μA
I_I	$V_I = V_{CC}$ or 0 V				±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or 0 V, I_O = 0				8		160		80	μA
C_i	(except transceiver I/O pins)			3	10		10		10	pF

‡All typical values are at V_{CC} = 5 V.
§This parameter, I_{OZ}, the high impedance-state output current, applies only for three-state outputs and transceiver I/O pins.

switching characteristics

See individual circuit pages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} ..... −0.5 to 7 V
Input diode current, I_{IK}($V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
Output diode current, I_{OK}($V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±20 mA
Continuous output current ($-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$) ..... ±25 mA
Continuous current through V_{CC} or GND pins ..... ±50 mA
Lead temperature 1,6 mm (1/16 in) from case: J package for 60 seconds ..... 300°C
N package for 10 seconds ..... 260°C
Storage temperature range ..... −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC'			SN74HC'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		2	5	6	2	5	6	V
V_{IH} High-level input voltage	V_{CC} = 4.5 V	3.15			3.15			V
	V_{CC} = 5 V	3.50			3.50			
	V_{CC} = 5.5 V	3.85			3.85			
V_{IL} Low-level input voltage	V_{CC} = 4.5 V	0		0.9	0		0.9	V
	V_{CC} = 5 V	0		1.0	0		1.0	
	V_{CC} = 5.5 V	0		1.1	0		1.1	
V_I Input voltage		−0.5		V_{CC} + 0.5	−0.5		V_{CC} + 0.5	V
V_O Output voltage		−0.5		V_{CC} + 0.5	−0.5		V_{CC} + 0.5	V
I_{OH} High-level output current				−4			−4	mA
I_{OL} Low-level output current				3.4			4	mA
t_t Input transition (rise and fall) times (except Schmitt-trigger inputs)		0		500	0		500	ns
T_A Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics, V_{CC} = 5 V ± 10%, over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54HC'		SN74HC'		UNIT
			MIN	TYP‡	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}, V_{CC} = 4.5 V, I_{OH} = −4mA		3.86			3.56		3.70		V
	$V_I = V_{IH}$ or V_{IL}, I_{OH} = −200 μA		V_{CC} −0.2	V_{CC}		V_{CC} −0.2		V_{CC} −0.2		
	$V_I = V_{IH}$ or V_{IL}, I_{OH} = −20 μA		V_{CC} −0.1	V_{CC}		V_{CC} −0.1		V_{CC} −0.1		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 3.4 mA			0.27		0.4			V
		I_{OL} = 4 mA			0.32				0.4	
	$V_I = V_{IH}$ or V_{IL}, I_{OL} = 20 μA			0	0.1		0.1		0.1	
$V_{T+} - V_{T-}$¶			0.4	1		0.4		0.4		V
I_I	$V_I = V_{CC}$ or 0 V, I_o = 0				±0.1		±1		±1	μA
I_{CC}	$V_I = V_{CC}$ or 0 V				8		160		80	μA
C_i				3	10		10		10	pF

‡All typical values are at V_{CC} = 5 V. ¶This parameter applies only to Schmitt-trigger inputs.

switching characteristics

See individual circuit pages.

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Descriptive Information

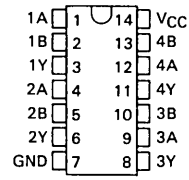
3

TYPES SN54HC00, SN74HC00 QUADRUPLE 2-INPUT POSITIVE-NAND GATES

D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC00 . . . J PACKAGE
SN74HC00 . . . J OR N PACKAGE
(TOP VIEW)



description

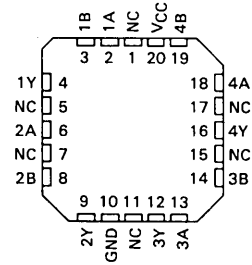
These devices contain four independent 2-input NAND gates. They perform the boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN54HC00 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC00 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE (each gate)

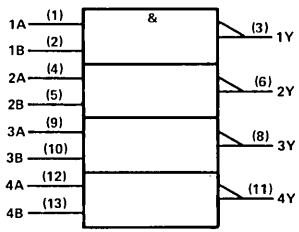
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

SN54HC00 . . . FH OR FK PACKAGE
SN74HC00 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics.

See Table I, page 2-3.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF				UNIT
						T_A = 25°C		SN54HC00	SN74HC00	
			MIN	TYP	MAX	MIN	TYP MAX	MIN MAX	MIN MAX	
t_{PLH}	A or B	Y								ns
t_{PHL}										

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TYPES SN54HC02, SN74HC02
QUADRUPLE 2-INPUT POSITIVE-NOR GATES

D2684, DECEMBER 1982

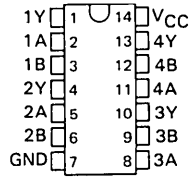
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

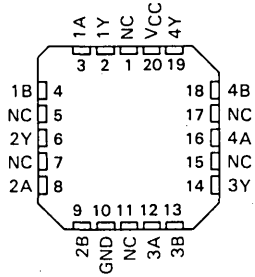
These devices contain four independent 2-input NOR gates. They perform the boolean functions $Y = \overline{A + B}$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

The SN54HC02 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC02 is characterized for operation from −40°C to 85°C.

SN54HC02 . . . J PACKAGE
SN74HC02 . . . J OR N PACKAGE
(TOP VIEW)

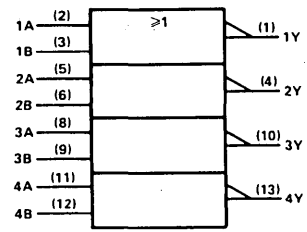


SN54HC02 . . . FH OR FK PACKAGE
SN74HC02 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

logic symbol



Pin numbers shown are for J and N packages.

FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

maximum ratings, recommended operating conditions, and electrical characteristics

See Table I, page 2-3.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF				UNIT
						T_A = 25°C		SN54HC02	SN74HC02	
			MIN	TYP	MAX	MIN	TYP MAX	MIN MAX	MIN MAX	
t_{PLH}	A or B	Y								ns
t_{PHL}										

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

PRODUCT PREVIEW

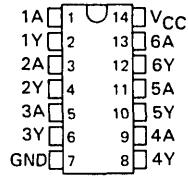
This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TYPES SN54HC04, SN74HC04
HEX INVERTERS

D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC04 . . . J PACKAGE
SN74HC04 . . . J OR N PACKAGE
(TOP VIEW)

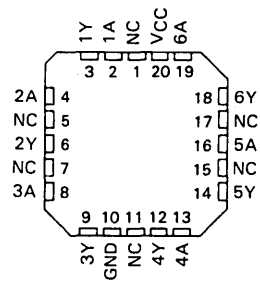


description

These devices contain six independent inverters. They perform the boolean function $Y = \overline{A}$.

The SN54HC04 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC04 is characterized for operation from −40°C to 85°C.

SN54HC04 . . . FH OR FK PACKAGE
SN74HC04 . . . FH OR FN PACKAGE
(TOP VIEW)

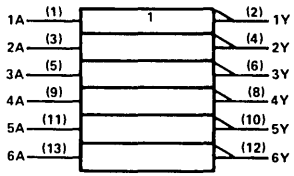


NC — No internal connection

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table I, page 2-3.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF						UNIT
						T_A = 25°C			SN54HC04		SN74HC04	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y											ns
t_{PHL}													

C_{pd}	Power dissipation capacitance per inverter	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

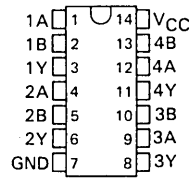
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TYPES SN54HC08, SN74HC08
QUADRUPLE 2-INPUT POSITIVE-AND GATES

D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC08 . . . J PACKAGE
SN74HC08 . . . J OR N PACKAGE
(TOP VIEW)

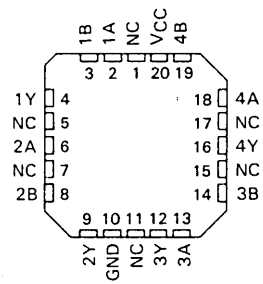


description

These devices contain four independent 2-input AND gates. They perform the boolean functions $Y = A \cdot B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic.

The SN54HC08 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC08 is characterized for operation from −40°C to 85°C.

SN54HC08 . . . FH OR FK PACKAGE
SN74HC08 . . . FH OR FN PACKAGE
(TOP VIEW)

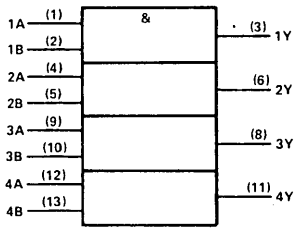


NC — No internal connection

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table I, page 2-3.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF				UNIT
						T_A = 25°C		SN54HC08	SN74HC08	
			MIN	TYP	MAX	MIN	TYP MAX	MIN MAX	MIN MAX	
t_{PLH}	A or B	Y								ns
t_{PHL}										

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

PRODUCT PREVIEW

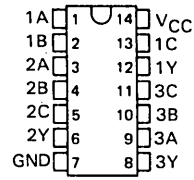
This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TYPES SN54HC10, SN74HC10
TRIPLE 3-INPUT POSITIVE-NAND GATES

D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC10 . . . J PACKAGE
SN74HC10 . . . J OR N PACKAGE
(TOP VIEW)

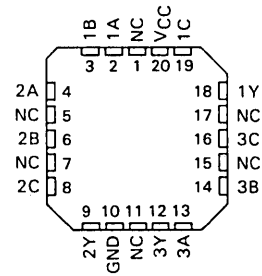


description

These devices contain three independent 3-input NAND gates. They perform the boolean functions $Y = \overline{A \cdot B \cdot C}$ or $Y = \overline{A} + \overline{B} + \overline{C}$ in positive logic.

The SN54HC10 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC10 is characterized for operation from −40°C to 85°C.

SN54HC10 . . . FH OR FK PACKAGE
SN74HC10 . . . FH OR FN PACKAGE
(TOP VIEW)

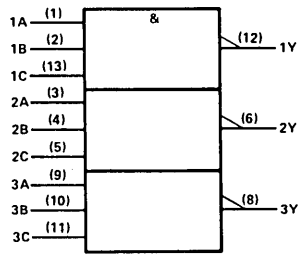


NC — No internal connection

FUNCTION TABLE (each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table I, page 2-3.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF						UNIT
						T_A = 25°C			SN54HC10		SN74HC10	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	MIN	MAX
t_{PLH}	A, B, or C	Y										ns
t_{PHL}												

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

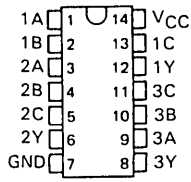
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TYPES SN54HC11, SN74HC11
TRIPLE 3-INPUT POSITIVE-AND GATES

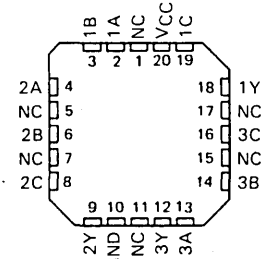
D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC11 . . . J PACKAGE
SN74HC11 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC11 . . . FH OR FK PACKAGE
SN74HC11 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

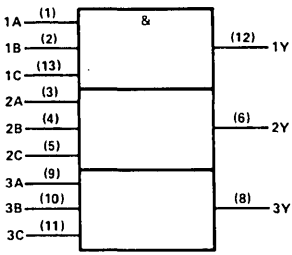
These devices contain three independent 3-input AND gates. They perform the boolean functions $Y = A \cdot B \cdot C$ or $Y = \overline{\overline{A} + \overline{B} + \overline{C}}$ in positive logic.

The SN54HC11 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC11 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE (each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table I, page 2-3.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF						UNIT
						T_A = 25°C			SN54HC11		SN74HC11	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	MIN	MAX
t_{PLH}	A, B, or C	Y										ns
t_{PHL}												

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	pF typ

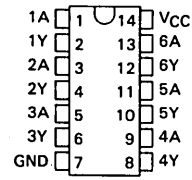
NOTE 1: For load circuit and voltage waveforms, see page 1-14.

TYPES SN54HC14, SN74HC14
HEX SCHMITT-TRIGGER INVERTERS

D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC14 . . . J PACKAGE
SN74HC14 . . . J OR N PACKAGE
(TOP VIEW)



description

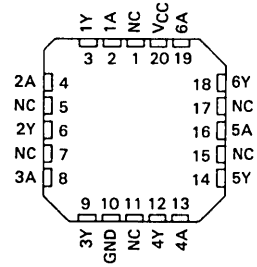
These Schmitt-trigger devices contain six independent inverters. They perform the boolean function Y = A.

The SN54HC14 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74HC14 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE
(each inverter)

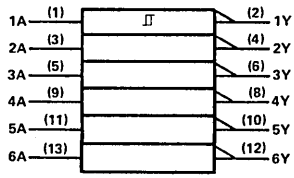
INPUT A	OUTPUT Y
H	L
L	H

SN54HC14 . . . FH OR FK PACKAGE
SN74HC14 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table I, page 2-3.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF						UNIT
						T_A = 25°C			SN54HC14		SN74HC14	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y											ns
t_{PHL}	A	Y											ns

C_{pd}	Power dissipation capacitance per inverter	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TYPES SN54HC20, SN74HC20 DUAL 4-INPUT POSITIVE-NAND GATES

D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

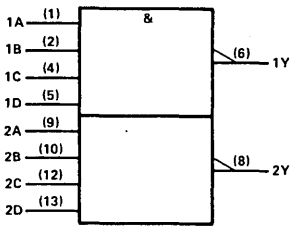
These devices contain two independent 4-input NAND gates. They perform the boolean functions $Y = \overline{A \cdot B \cdot C \cdot D}$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$ *in positive logic.*

The SN54HC20 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC20 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE (each gate)

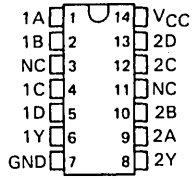
INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

logic symbol

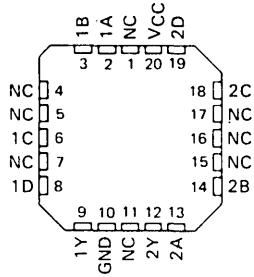


Pin numbers shown are for J and N packages.

SN54HC20 . . . J PACKAGE
SN74HC20 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC20 . . . FH OR FK PACKAGE
SN74HC20 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

maximum ratings, recommended operating conditions, and electrical characteristics

See Table I, page 2-3.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF				UNIT
						T_A = 25°C			SN54HC20	SN74HC20	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN MAX	MIN MAX	
t_{PLH}	A, B, C, or D	Y									ns
t_{PHL}											

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	pF typ

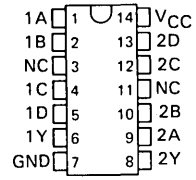
NOTE 1: For load circuit and voltage waveforms, see page 1-14.

TYPES SN54HC21, SN74HC21
DUAL 4-INPUT POSITIVE-AND GATES

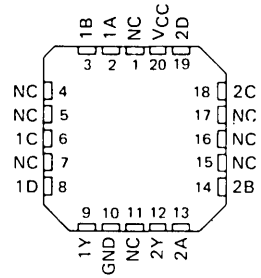
D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC21 . . . J PACKAGE
SN74HC21 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC21 . . . FH OR FK PACKAGE
SN74HC21 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

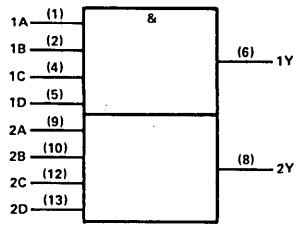
These devices contain two independent 4-input AND gates. They perform the boolean functions $Y = A \cdot B \cdot C \cdot D$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$ in positive logic.

The SN54HC21 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC21 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE (each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	H
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table I, page 2-3.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF				UNIT
						T_A = 25°C		SN54HC21	SN74HC21	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN MAX	MIN MAX	
t_{PLH}	A, B, C, or D	Y									ns
t_{PHL}											

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

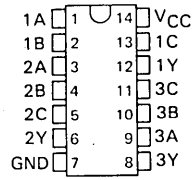
TYPES SN54HC27, SN74HC27
TRIPLE 3-INPUT POSITIVE-NOR GATES

D2684, DECEMBER 1982

Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs

Dependable Texas Instruments Quality and Reliability

SN54HC27 . . . J PACKAGE
SN74HC27 . . . J OR N PACKAGE
(TOP VIEW)

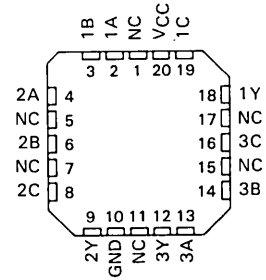


description

These devices contain three independent 3-input NOR gates. They perform the boolean functions $Y = \overline{A + B + C}$ or $Y = \overline{A} \cdot \overline{B} \cdot \overline{C}$ in positive logic.

The SN54HC27 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC27 is characterized for operation from −40°C to 85°C.

SN54HC27 . . . FH OR FK PACKAGE
SN74HC27 . . . FH OR FN PACKAGE
(TOP VIEW)

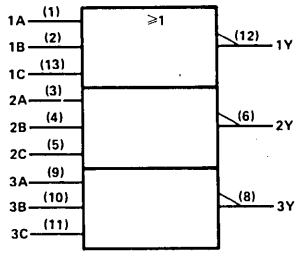


NC — No internal connection

FUNCTION TABLE (each gate)

INPUTS			OUTPUT
A	B	C	Y
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table I, page 2-3.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF				UNIT
						T_A = 25°C		SN54HC27	SN74HC27	
			MIN	TYP	MAX	MIN	TYP MAX	MIN MAX	MIN MAX	
t_{PLH}	A, B, or C	Y								ns
t_{PHL}										

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

PRODUCT PREVIEW

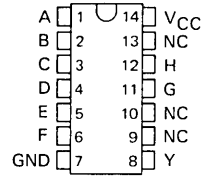
This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TYPES SN54HC30, SN74HC30
8-INPUT POSITIVE-NAND GATES

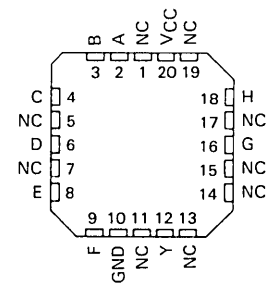
D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC30 . . . J PACKAGE
SN74HC30 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC30 . . . FH OR FK PACKAGE
SN74HC30 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

These devices contain a single 8-input NAND gate and perform the following boolean functions in positive logic:

$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H}$$

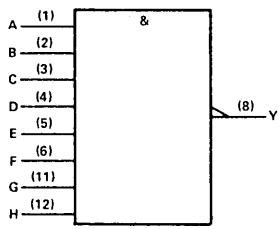
or

$$Y = \bar{A} + \bar{B} + \bar{C} + \bar{D} + \bar{E} + \bar{F} + \bar{G} + \bar{H}$$

The SN54HC30 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC30 is characterized for operation from −40°C to 85°C.

3

logic symbol



Pin numbers shown are for J and N packages.

FUNCTION TABLE

INPUTS A THRU H	OUTPUT Y
All inputs H	L
One or more inputs L	H

maximum ratings, recommended operating conditions, and electrical characteristics

See Table I, page 2-3.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF				UNIT
						T_A = 25°C		SN54HC30	SN74HC30	
			MIN	TYP	MAX	MIN	TYP MAX	MIN MAX	MIN MAX	
t_{PLH}	A thru H	Y								ns
t_{PHL}										

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

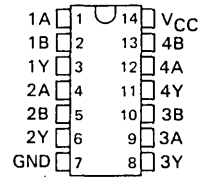
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TYPES SN54HC32, SN74HC32 QUADRUPLE 2-INPUT POSITIVE-OR GATES

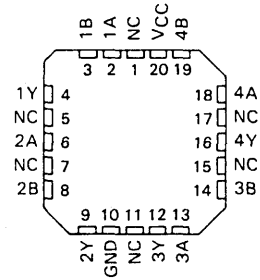
D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC32 . . . J PACKAGE
SN74HC32 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC32 . . . FH OR FK PACKAGE
SN74HC32 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

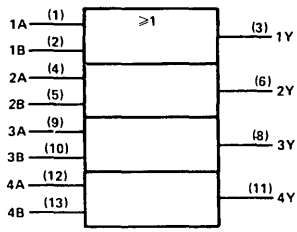
These devices contain four independent 2-input OR gates. They perform the boolean functions $Y = A + B$ or $Y = \overline{\overline{A} \cdot \overline{B}}$ in positive logic.

The SN54HC32 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC32 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table I, page 2-3.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF						UNIT
						T_A = 25°C			SN54HC32		SN74HC32	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y											ns
t_{PHL}													

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

PRODUCT PREVIEW

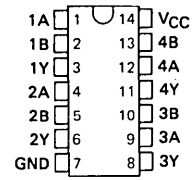
This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TYPES SN54HC36, SN74HC36 QUADRUPLE 2-INPUT POSITIVE-NOR GATES

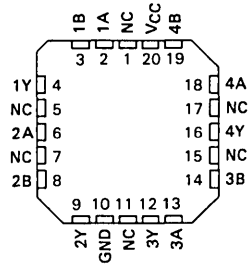
D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC36 . . . J PACKAGE
SN74HC36 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC36 . . . FH OR FK PACKAGE
SN74HC36 . . . FH OR FN PACKAGE
(TOP VIEW)



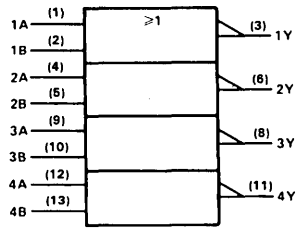
NC — No internal connection

description

These devices contain four independent 2-input NOR gates. They perform the boolean functions $Y = \overline{A + B}$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

The SN54HC36 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC36 is characterized for operation from −40°C to 85°C.

logic symbol



Pin numbers shown are for J and N packages.

FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

maximum ratings, recommended operating conditions, and electrical characteristics

See Table I, page 2-3.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF				UNIT
						T_A = 25°C		SN54HC36	SN74HC36	
			MIN	TYP	MAX	MIN	TYP MAX	MIN MAX	MIN MAX	
t_{PLH}	A or B	Y								ns
t_{PHL}										

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

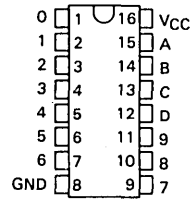
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TYPES SN54HC42, SN74HC42
4-LINE TO 10-LINE DECODERS (1-of-10)

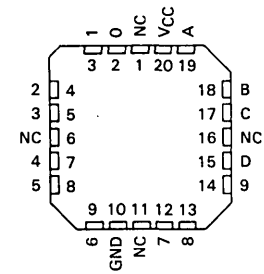
D2684, DECEMBER 1982

- **Full Decoding of Input Logic**
- **All Outputs Are Off for Invalid BCD Conditions**
- **Also for Application as 3-Line to 8-Line Decoders**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC42 . . . J PACKAGE
SN74HC42 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC42 . . . FH OR FK PACKAGE
SN74HC42 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

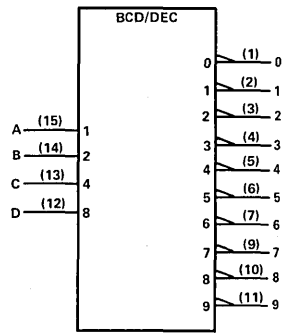
These monolithic decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all inputs remain off for all invalid input conditions.

The SN54HC42 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC42 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

NO.	INPUTS				OUTPUTS									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table IV, page 2-6.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF				UNIT
						T_A = 25°C		SN54HC42	SN74HC42	
			MIN	TYP	MAX	MIN	TYP MAX	MIN MAX	MIN MAX	
t_{PHL}	A,B,C or D	0 thru 9								ns
t_{PLH}										

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

3

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TYPES SN54HC51, SN74HC51
AND-OR-INVERT GATES

D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

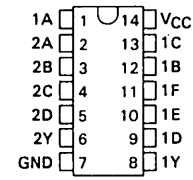
The 'HC51 provides 2-wide, 2-input, and 2-wide, 3-input AND-OR-INVERT gates. The device performs the following boolean functions:

$$1Y = \overline{(1A \cdot 1B \cdot 1C) + (1D \cdot 1E \cdot 1F)}$$

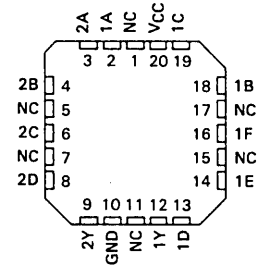
$$2Y = \overline{(2A \cdot 2B \cdot) + (2C \cdot 2D)}$$

The SN54HC51 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC51 is characterized for operation from −40°C to 85°C.

SN54HC51 . . . J PACKAGE
SN74HC51 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC51 . . . FH OR FK PACKAGE
SN74HC51 . . . FH OR FN PACKAGE
(TOP VIEW)



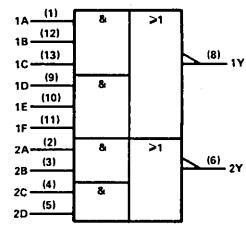
NC — No internal connection

FUNCTION TABLES

INPUTS						OUTPUT
1A	1B	1C	1D	1E	1F	1Y
H	H	H	X	X	X	L
X	X	X	H	H	H	L
Any other combination						H

INPUTS				OUTPUT
2A	2B	2C	2D	2Y
H	H	X	X	L
X	X	H	H	L
Any other combination				H

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table I, page 2-3.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF				UNIT
						T_A = 25°C		SN54HC51	SN74HC51	
			MIN	TYP	MAX	MIN	TYP MAX	MIN MAX	MIN MAX	
t_{PLH}	Any	Y								ns
t_{PHL}										

C_{pd}	Power dissipation capacitance per AOI gate	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

PRODUCT PREVIEW

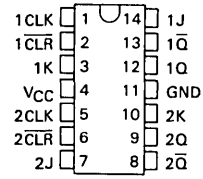
This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TYPES SN54HC73, SN74HC73
DUAL J-K FLIP-FLOPS WITH CLEAR

D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC73 . . . J PACKAGE
SN74HC73 . . . J OR N PACKAGE
(TOP VIEW)



For chip carrier information, contact the factory.

description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the clear input resets the outputs regardless of the levels of the other inputs. When clear is inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

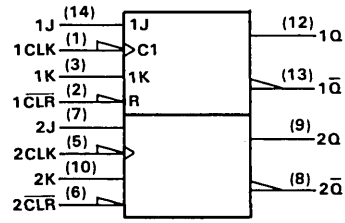
The SN54HC73 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC73 is characterized for operation from −40°C to 85°C.

3

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS				OUTPUTS	
$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\overline{Q}_0$

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table II, page 2-4.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

timing requirements (supplement to recommended operating conditions)

			SN54HC73			SN74HC73			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	CLK high or low							ns
		$\overline{CLR}$ low							
t_{su}	Setup time before CLK↓	High-level data							ns
		Low-level data							
		$\overline{CLR}$ inactive							
t_h	Hold time, data after CLK↓								ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF					UNIT
						T_A = 25°C			SN54HC73	SN74HC73	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN MAX	MIN MAX	
f_{max}											MHz
t_{PLH}	CLK	Q or $\overline{Q}$									ns
t_{PHL}											
t_{PLH}	$\overline{CLR}$	$\overline{Q}$									ns
t_{PHL}		Q									

C_{pd}	Power dissipation capacitance per flip-flop	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

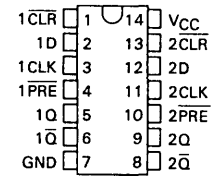
3

TYPES SN54HC74, SN74HC74
DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

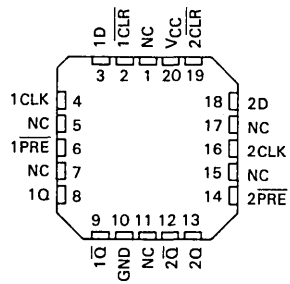
D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC74 . . . J PACKAGE
SN74HC74 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC74 . . . FH OR FK PACKAGE
SN74HC74 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high) data at the D input meeting the setup time requirements are transferred to the outputs on the the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

The SN54HC74 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC74 is characterized for operation from −40°C to 85°C.

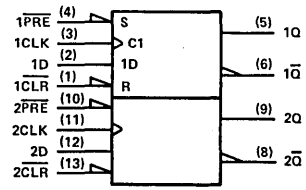
3

FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	Q_0

†This configuration is nonstable; that is, it will not persist when Preset or Clear returns to its inactive (high) level.

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table II, page 2-4.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

timing requirements (supplement to recommended operating conditions)

			SN54HC74			SN74HC74			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low							ns
		CLK high							
		CLK low							
t_{su}	Setup time before CLK↑	Data							ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive							
t_h	Hold time, data after CLK↑								ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF					UNIT
						T_A = 25°C			SN54HC74	SN74HC74	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN MAX	MIN MAX	
f_{max}											MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$									ns
t_{PHL}											
t_{PLH}	CLK	Q or $\overline{Q}$									ns
t_{PHL}											

C_{pd}	Power dissipation capacitance per flip-flop	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

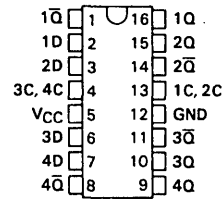
3

TYPES SN54HC75, SN74HC75
4-BIT BISTABLE LATCHES

D2684, DECEMBER 1982

- **Complementary Q and $\overline{Q}$ Outputs**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC75 . . . J PACKAGE
SN74HC75 . . . J OR N PACKAGE
(TOP VIEW)



description

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (C) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

The SN54HC75 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC75 is characterized for operation from −40°C to 85°C.

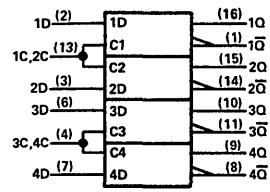
For chip carrier information, contact the factory

3

FUNCTION TABLE
(Each Latch)

INPUTS		OUTPUTS	
D	C	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table II, page 2-4.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

timing requirements (supplement to recommended operating conditions)

		SN54HC75			SN74HC75			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
t_w	Pulse duration, C high							ns
t_{su}	Setup time, data before Cl							ns
t_h	Hold time, data after Cl							ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF				UNIT
						T_A = 25°C		SN54HC75	SN74HC75	
			MIN	TYP	MAX	MIN	TYP MAX	MIN MAX	MIN MAX	
t_{PLH}	D	Q								ns
t_{PHL}										
t_{PLH}	D	$\overline{Q}$								ns
t_{PHL}										
t_{PLH}	C	Q								ns
t_{PHL}										
t_{PLH}	C	$\overline{Q}$								ns
t_{PHL}										

C_{pd}	Power dissipation capacitance per latch	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

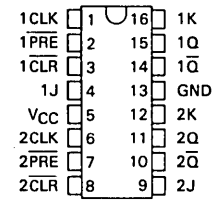
3

TYPES SN54HC76, SN74HC76
DUAL J-K FLIP-FLOPS WITH CLEAR AND PRESET

D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC76 . . . J PACKAGE
SN74HC76 . . . J OR N PACKAGE
(TOP VIEW)



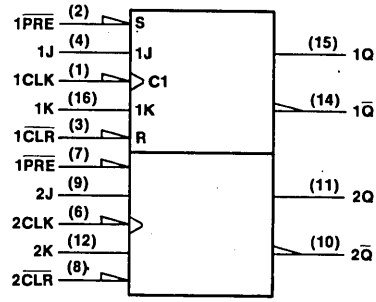
For chip carrier information, contact the factory.

description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the Preset or Clear input sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can also perform as toggle flip-flops by tying J and K high.

The SN54HC76 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC76 is characterized for operation from −40°C to 85°C.

logic symbol



Pin numbers shown are for J and N packages.

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

*This configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table II, page 2-4.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

timing requirements (supplement to recommended operating conditions)

			SN54HC76			SN74HC76			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low							ns
		CLK high							
		CLK low							
t_{su}	Setup time before CLK↓	Data							ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive							
t_h	Hold time, data after CLK↓								ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF						UNIT
						T_A = 25°C			SN54HC76		SN74HC76	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	MIN	MAX
f_{max}												MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$										ns
t_{PHL}												
t_{PLH}	CLK	Q or $\overline{Q}$										ns
t_{PHL}												

C_{pd}	Power dissipation capacitance per flip-flop	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

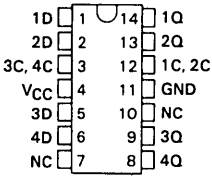
3

TYPES SN54HC77, SN74HC77
4-BIT BISTABLE LATCHES

D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC77 . . . J PACKAGE
SN74HC77 . . . J OR N PACKAGE
(TOP VIEW)



NC — No internal connection

For chip carrier information, contact the factory.

description

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (C) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

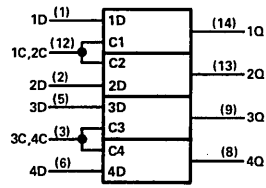
The SN54HC77 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC77 is characterized for operation from −40°C to 85°C.

3

FUNCTION TABLE
(Each Latch)

INPUTS		OUTPUT
D	C	Q
L	H	L
H	H	H
X	L	Q_0

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table II, page 2-4.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

timing requirements (supplement to recommended operating conditions)

		SN54HC77			SN74HC77			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
t_w	Pulse duration, C high							ns
t_{su}	Setup time, data before C↓							ns
t_h	Hold time, data after C↓							ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF				UNIT
						T_A = 25°C		SN54HC77	SN74HC77	
			MIN	TYP	MAX	MIN	TYP MAX	MIN MAX	MIN MAX	
t_{PLH}	D	Q								ns
t_{PHL}										
t_{PLH}	C	Q								ns
t_{PHL}										

C_{pd}	Power dissipation capacitance per latch	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

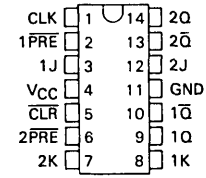
3

TYPES SN54HC78, SN74HC78
DUAL J-K FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC78 . . . J PACKAGE
SN74HC78 . . . J OR N PACKAGE
(TOP VIEW)



For chip carrier information, contact the factory.

description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the Preset or Clear input sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can also perform as toggle flip-flops by tying J and K high.

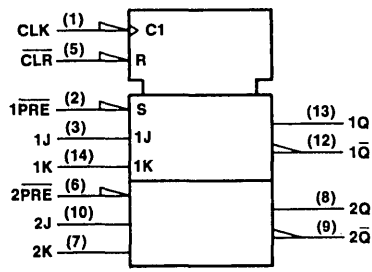
The SN54HC78 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC78 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

*This configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table II, page 2-4.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

timing requirements (supplement to recommended operating conditions)

			SN54HC78			SN74HC78			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low							ns
		CLK high							
		CLK low							
t_{su}	Setup time before CLK↓	Data							ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive							
t_h	Hold time, data after CLK↓								ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF				UNIT
						T_A = 25°C		SN54HC78	SN74HC78	
			MIN	TYP	MAX	MIN	TYP MAX	MIN MAX	MIN MAX	
f_{max}										MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$								ns
t_{PHL}										
t_{PLH}	CLK	Q or $\overline{Q}$								ns
t_{PHL}										

C_{pd}	Power dissipation capacitance per flip-flop	No load, T_A = 25°C	pF typ

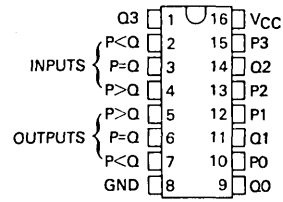
NOTE 1: For load circuit and voltage waveforms, see page 1-14.

TYPES SN54HC85, SN74HC85
4-BIT MAGNITUDE COMPARATORS

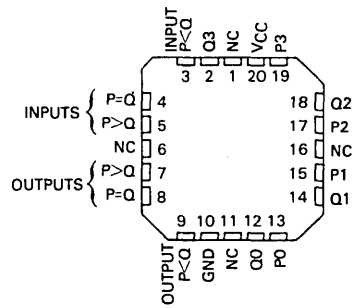
D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC85 . . . J PACKAGE
SN74HC85 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC85 . . . FH OR FK PACKAGE
SN74HC85 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

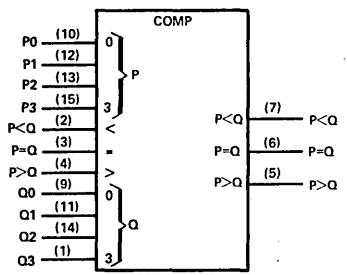
These four-bit magnitude comparators perform comparison of straight binary and straight BCD (8-4-2-1) codes. Three fully decoded decisions about two 4-bit words (P, Q) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The P > Q, P < Q, and P = Q outputs of a stage handling less-significant bits are connected to the corresponding P > Q, P < Q, and P = Q inputs of the next state handling more-significant bits. The stage handling the least-significant bits must have a high-level voltage applied to the P = Q input. The cascading path of the 'HC85 is implemented with only a two-gate-level delay to reduce overall comparison times for long words.

The SN54HC85 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74HC85 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
P3, Q3	P2, Q2	P1, Q1	P0, Q0	P > Q	P < Q	P = Q	P > Q	P < Q	P = Q
P3 = Q3	P2 = Q2	P1 = Q1	P0 = Q0	X	X	H	L	L	H
P3 = Q3	P2 = Q2	P1 = Q1	P0 = Q0	H	H	L	L	L	L
P3 = Q3	P2 = Q2	P1 = Q1	P0 = Q0	L	L	L	H	H	L

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table IV, page 2-6.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF						UNIT
						T_A = 25°C			SN54HC85		SN74HC85	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any P or Q data input	P<Q, P>Q											ns
		P=Q											
t_{PHL}	Any P or Q data input	P<Q, P>Q											ns
		P=Q											
t_{PLH}	P<Q or P=Q	P>Q											ns
t_{PHL}													
t_{PLH}	P=Q	P=Q											ns
t_{PHL}													
t_{PLH}	P>Q or P=Q	P<Q											ns
t_{PHL}													

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

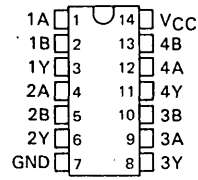
3

TYPES SN54HC86, SN74HC86
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

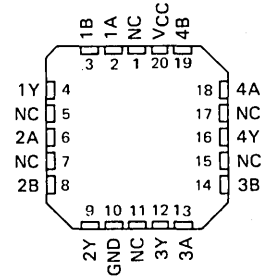
D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- ***Dependable Texas Instruments Quality and Reliability***

SN54HC86 . . . J PACKAGE
SN74HC86 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC86 . . . FH OR FK PACKAGE
SN74HC86 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

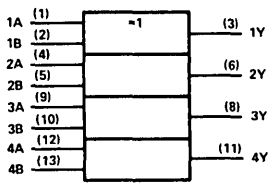
description

These devices contain four independent 2-input Exclusive-OR gates. They perform the boolean functions $Y = A \oplus B = \bar{A}B + A\bar{B}$ in positive logic.

A common application is as a true/complement element. If one of the inputs is low, the other input will be reproduced in true form at the output. If one of the inputs is high, the signal on the other input will be reproduced inverted at the output.

The SN54HC86 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74HC86 is characterized for operation from -40°C to 85°C.

logic symbol



Pin numbers shown are for J and N packages.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

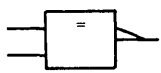
exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

EXCLUSIVE-OR

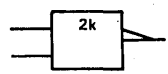
These are five equivalent Exclusive-OR symbols valid for an 'HC86 gate in positive logic; negation may be shown at any two ports.

LOGIC IDENTITY ELEMENT



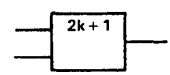
The output is active (low) if all inputs stand at the same logic level (i.e., A = B).

EVEN-PARITY



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table I, page 2-3.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF				UNIT
						T_A = 25°C		SN54HC86	SN74HC86	
			MIN	TYP	MAX	MIN	TYP MAX	MIN MAX	MIN MAX	
t_{PLH}	A or B (other input low)	Y								ns
t_{PHL}										
t_{PLH}	A or B (other input high)	Y								ns
t_{PLH}										

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see pages 1-14.

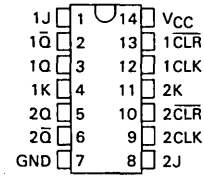
3

TYPES SN54HC107, SN74HC107
DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR

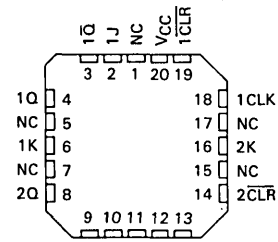
D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC107 . . . J PACKAGE
SN74HC107 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC107 . . . FH OR FK PACKAGE
SN74HC107 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

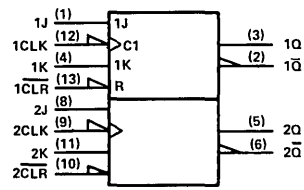
These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the $\overline{CLR}$ input resets the outputs regardless of the levels of the other inputs. When $\overline{CLR}$ is inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The SN54HC107 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC107 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\overline{Q}_0$

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table II, page 2-4.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

timing requirements (supplement to recommended operating conditions)

			SN54HC107			SN74HC107			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	$\overline{CLR}$ low							ns
		CLK high							
		CLK low							
t_{su}	Setup time before CLK↓	Data							ns
		$\overline{CLR}$ inactive							
t_h	Hold time, data after CLK↓								ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF					UNIT
						T_A = 25°C			SN54HC107	SN74HC107	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN MAX	MIN MAX	
f_{max}											MHz
t_{PLH}	$\overline{CLR}$	Q or $\overline{Q}$									ns
t_{PHL}											
t_{PLH}	CLK	Q or $\overline{Q}$									ns
t_{PHL}											

C_{pd}	Power dissipation capacitance per flip-flop	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

3

TYPES SN54HC109, SN74HC109
DUAL J-$\overline{K}$ POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

D2684, DECEMBER 1982

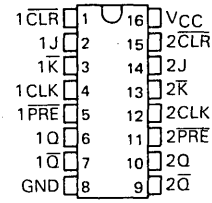
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

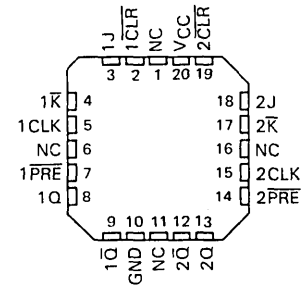
These devices contain two independent J-$\overline{K}$ positive-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the J and $\overline{K}$ inputs meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and $\overline{K}$ inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding $\overline{K}$ and tying J high. They also can perform as D-type flip-flops if J and $\overline{K}$ are tied together.

The SN54HC109 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC109 is characterized for operation from −40°C to 85°C.

SN54HC109 . . . J PACKAGE
SN74HC109 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC109 . . . FH OR FK PACKAGE
SN74HC109 . . . FH OR FN PACKAGE
(TOP VIEW)



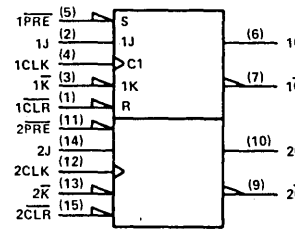
NC — No Internal connection

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

*This configuration is nonstable; that is, it will not persist when Preset or Clear return to their inactive (high) level.

logic symbol



Pin numbers shown are for J and N packages

maximum ratings, recommended operating conditions, and electrical characteristics.

See Table II, page 2-4.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

timing requirements (supplement to recommended operating conditions)

			SN54HC109			SN74HC109			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low							ns
		CLK high							
		CLK low							
t_{su}	Setup time before CLK↑	Data							ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive							
t_h	Hold time, data after CLK↑								ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF					UNIT
						T_A = 25°C			SN54HC109	SN74HC109	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN MAX	MIN MAX	
f_{max}											MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$									ns
t_{PHL}											
t_{PLH}	CLK	Q or $\overline{Q}$									ns
t_{PHL}											

C_{pd}	Power dissipation capacitance per flip-flop	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

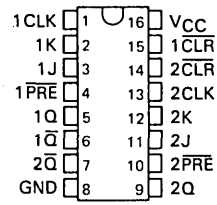
3

TYPES SN54HC112, SN74HC112 DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

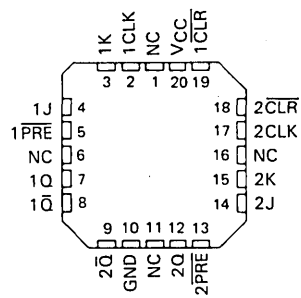
D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC112 . . . J PACKAGE
SN74HC112 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC112 . . . FH OR FK PACKAGE
SN74HC112 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The SN54HC112 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC112 is characterized for operation from −40°C to 85°C.

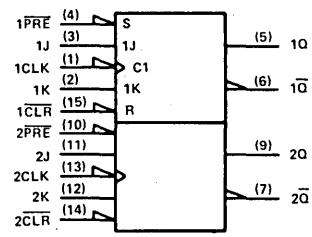
3

FUNCTION TABLE

INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

*This configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table II, page 2-4.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

timing requirements (supplement to recommended operating conditions)

			SN54HC112			SN74HC112			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low							ns
		CLK high							
		CLK low							
t_{su}	Setup time before CLK↓	Data							ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive							
t_h	Hold time, data after CLK↓								ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF					UNIT
						T_A = 25°C			SN54HC112	SN74HC112	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN MAX	MIN MAX	
f_{max}											MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$									ns
t_{PHL}											
t_{PLH}	CLK	Q or $\overline{Q}$									ns
t_{PHL}											

C_{pd}	Power dissipation capacitance per flip-flop	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

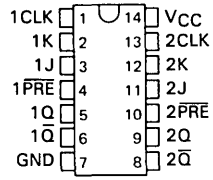
TYPES SN54HC113, SN74HC113
DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET

D2684, DECEMBER 1982

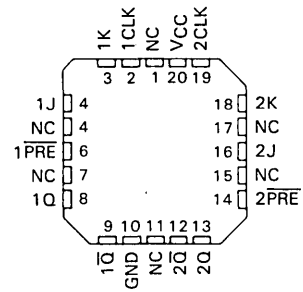
Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs

Dependable Texas Instruments Quality and Reliability

SN54HC113 . . . J PACKAGE
SN74HC113 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC113 . . . FH OR FK PACKAGE
SN74HC113 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

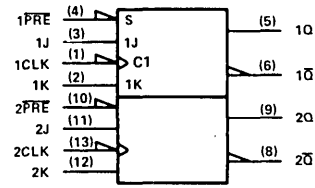
These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the Preset input sets the outputs regardless of the levels of the other inputs. When Preset ($\overline{PRE}$) is inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The SN54HC113 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC113 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{PRE}$	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	H	L
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\overline{Q}_0$

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table II, page 2-4.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

timing requirements (supplement to recommended operating conditions)

			SN54HC113			SN74HC113			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	$\overline{PRE}$ low							ns
		CLK high							
		CLK low							
t_{su}	Setup time before CLK ↓	Data							ns
		$\overline{PRE}$ inactive							
t_h	Hold time, data after CLK ↓								ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF					UNIT
						T_A = 25°C			SN54HC113	SN74HC113	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN MAX	MIN MAX	
f_{max}											
t_{PLH}	$\overline{PRE}$	Q or $\overline{Q}$									ns
t_{PHL}											
t_{PLH}	CLK	Q or $\overline{Q}$									ns
t_{PHL}											

C_{pd}	Power dissipation capacitance per flip-flop	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

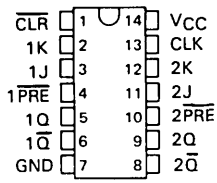
3

TYPES SN54HC114, SN74HC114
DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

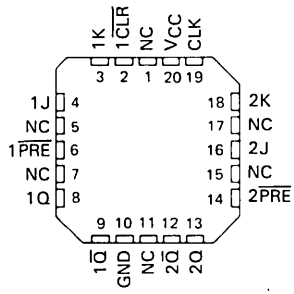
D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC114 . . . J PACKAGE
SN74HC114 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC114 . . . FH OR FK PACKAGE
SN74HC114 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The SN54HC114 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC114 is characterized for operation from −40°C to 85°C.

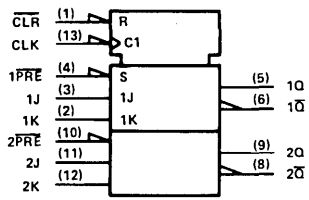
3

FUNCTION TABLE

INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

*This configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table II, page 2-4.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
INCORPORATED
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timing requirements (supplement to recommended operating conditions)

			SN54HC114			SN74HC114			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$							ns
		CLK high							
		CLK low							
t_{su}	Setup time before CLK ↓	Data							ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive							
t_h	Hold time, data after CLK ↓								ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF					UNIT
						T_A = 25°C			SN54HC114	SN74HC114	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN MAX	MIN MAX	
f_{max}											MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$									ns
t_{PHL}											
t_{PLH}	CLK	Q or $\overline{Q}$									ns
t_{PHL}											

C_{pd}	Power dissipation capacitance per flip-flop	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

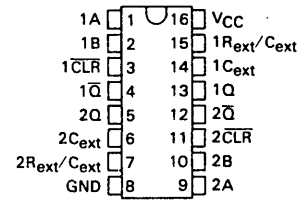
3

TYPES SN54HC123, SN74HC123
RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

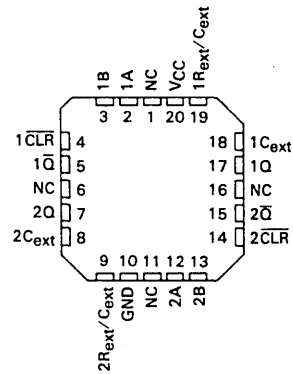
D2684, DECEMBER 1982

- **D-C Triggered by Active-High or Active-Low Inputs**
- **Retriggerable for Very Long Output Pulses, Up to 100% Duty Cycle**
- **Overriding Clear Terminates Output Pulse**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC123 . . . J PACKAGE
SN74HC123 . . . J OR N PACKAGE



SN54HC123 . . . FH or FK PACKAGE
SN74HC123 . . . FH or FN PACKAGE



description

These d-c triggered multivibrators feature output pulse duration control by three methods. The basic pulse duration is programmed by selection of external resistance and capacitance values. Once triggered, the basic pulse duration may be extended by retriggering the gated low-level-active (A) or high-level-active (B) inputs, or be reduced by use of the overriding clear. Figure 1 illustrates pulse control by retriggering and early clear.

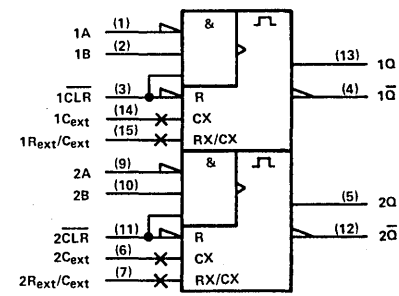
The SN54HC123 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74HC123 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L†	H†
X	X	L	L†	H†
H	L	↑	⎍	⎍
H	↓	H	⎍	⎍
↑	L	H	⎍	⎍

†The second and third lines each indicate the logic levels the outputs will take on after the completion of any pulse already started.

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table IV, page 2-6.

Note: The minimum recommended supply voltage for this device is 3 V.

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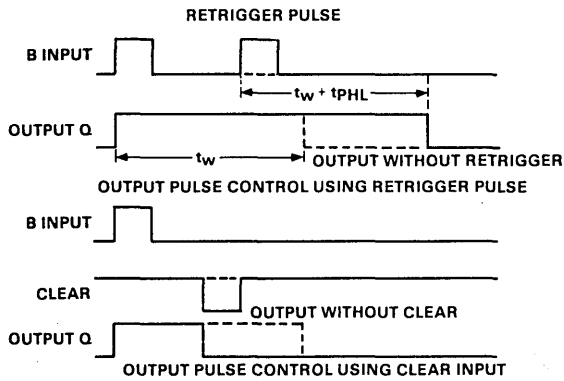


FIGURE 1 — TYPICAL INPUT/OUTPUT PULSES

3

timing requirements (supplement to recommended operating conditions)

		SN54HC123			SN74HC123			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
t_w	Pulse duration, A low, B high, or $\overline{CLR}$ low							ns
R_{ext}	External timing resistance							kΩ
C_{ext}	External timing capacitance							μF
	Wiring capacitance at R_{ext}/C_{ext} terminal							pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF						UNIT
						T_A = 25°C			SN54HC123		SN74HC123	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	MIN	MAX
t_{PLH}†	A	Q										ns
	B											
t_{PHL}†	A	$\overline{Q}$										ns
	B											
t_{PHL}†	$\overline{CLR}$	Q										ns
t_{PLH}†		$\overline{Q}$										
t_{wQ}(min)†	A or B	Q										ns
t_{wQ}‡	A or B	Q										μs

C_{pd}	Power dissipation capacitance per monostable	No load, T_A = 25°C	pF typ

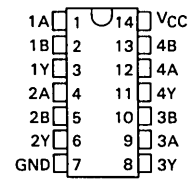
†C_{ext} = 0, R_{ext} = 5kΩ
‡t_{wQ} = duration of pulse at output Q. C_{ext} = 400 pF, R_{ext} = 10kΩ.
NOTE 1: For load circuit and voltage waveforms, see page 1-14.

TYPES SN54HC132, SN74HC132
SCHMITT-TRIGGER POSITIVE-NAND GATES
WITH TOTEM-POLE OUTPUTS

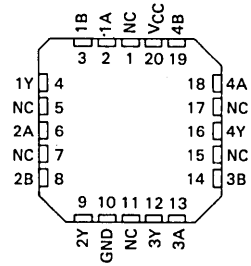
D2684, DECEMBER 1982

- **Operation from Very Slow Transitions**
- **Temperature-Compensated Threshold Levels**
- **High Noise Immunity**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC132 . . . J PACKAGE
SN74HC132 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC132 . . . FH OR FK PACKAGE
SN74HC132 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

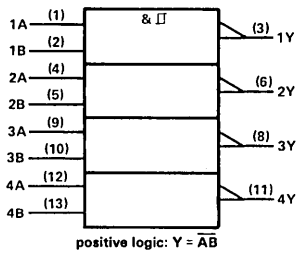
Each circuit functions as a NAND gate, but because of the Schmitt action, it has different input threshold levels for positive- and negative-going signals.

These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean jitter-free output signals.

The SN54HC132 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC132 is characterized for operation from −40°C to 85°C.

3

logic symbol



positive logic: $Y = \overline{AB}$

Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table I, page 2-3.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF						UNIT
						T_A = 25°C			SN54HC132		SN74HC132	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y											ns
t_{PHL}													

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
INCORPORATED
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TYPES SN54HC133, SN74HC133
13-INPUT POSITIVE-NAND GATES

D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

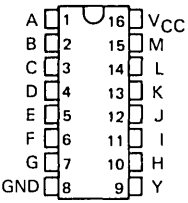
These devices contain a single 13-input NAND gate. They perform the boolean functions in positive logic:

$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H \cdot I \cdot J \cdot K \cdot L \cdot M} \quad \text{or}$$

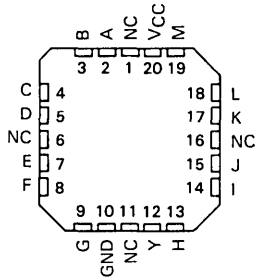
$$Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H} + \overline{I} + \overline{J} + \overline{K} + \overline{L} + \overline{M}$$

The SN54HC133 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC133 is characterized for operation from −40°C to 85°C.

SN54HC133 . . . J PACKAGE
SN74HC133 . . . J OR N PACKAGE
(TOP VIEW)

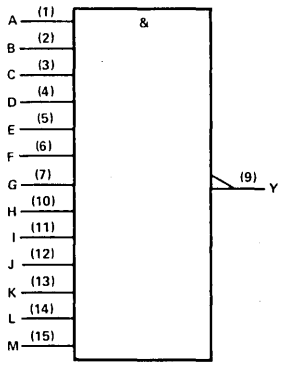


SN54HC133 . . . FH OR FK PACKAGE
SN74HC133 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

logic symbol



Pin numbers shown are for J and N packages.

FUNCTION TABLE

INPUTS A THRU M	OUTPUT Y
All inputs H	L
One or more inputs L	H

maximum ratings, recommended operating conditions, and electrical characteristics

See Table I, page 2-3.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF						UNIT
						T_A = 25°C			SN54HC133		SN74HC133	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y											ns
t_{PHL}													

C_{pd}	Power Dissipation capacitance per gate	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

PRODUCT PREVIEW

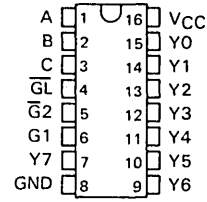
This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TYPES SN54HC137, SN74HC137
3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS WITH ADDRESS LATCHES

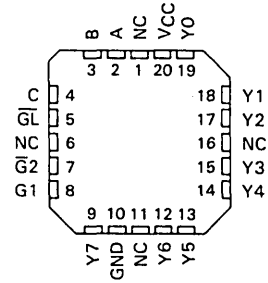
D2684, DECEMBER 1982

- **Combines Decoder and 3-Bit Address Latch**
- **Incorporates 2 Output Enables to Simplify Cascading**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC137 . . . J PACKAGE
SN74HC137 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC137 . . . FH OR FK PACKAGE
SN74HC137 . . . FH OR FN PACKAGE
(TOP VIEW)



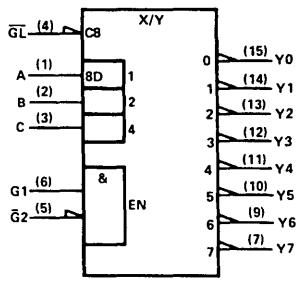
NC — No internal connection

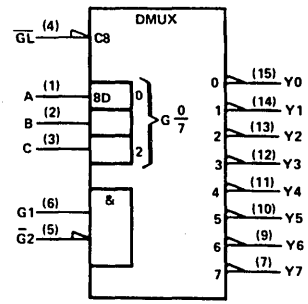
description

The 'HC137 is a three-line to eight-line decoder/demultiplexer with latches on the three address inputs. When the latch-enable input ($\overline{GL}$) is low, the 'HC137 acts as a decoder/demultiplexer. When $\overline{GL}$ goes from low to high, the address present at the select inputs (A, B, and C) is stored in the latches. Further address changes are ignored as long as $\overline{GL}$ remains high. The output enable controls, G1 and $\overline{G2}$, control the outputs independently of the select or latch-enable inputs. All of the outputs are forced high if G1 is low or $\overline{G2}$ is high. The 'HC137 is ideally suited for implementing glitch-free decoders in strobed (stored-address) applications in bus-oriented systems.

The SN54HC137 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC137 is characterized for operation from −40°C to 85°C.

logic symbols (alternatives)





Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table IV, page 2-6.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
INCORPORATED
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FUNCTION TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{GL}$	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Output corresponding to stored address, L; all others, H							

timing requirements (supplement to recommended operating conditions)

		SN54HC137			SN74HC137			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}	Clock frequency							MHz
t_w	Pulse duration, $\overline{GL}$ low							ns
t_{su}	Setup time, A, B, and C before $\overline{GL}$↑							ns
t_h	Hold time, A, B, and C after $\overline{GL}$↑							ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF					UNIT
						T_A = 25°C			SN54HC137	SN74HC137	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN MAX	MIN MAX	
f_{max}											MHz
t_{PLH}	A, B, C	Y									ns
t_{PHL}											
t_{PLH}	$\overline{G2}$	Y									ns
t_{PHL}											
t_{PLH}	G1	Y									ns
t_{PHL}											
t_{PLH}	$\overline{GL}$	Y									ns
t_{PHL}											

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	pF typ

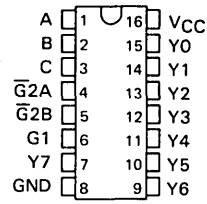
NOTE 1: For load circuit and voltage waveforms, see page 1-14.

TYPES SN54HC138, SN74HC138
3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

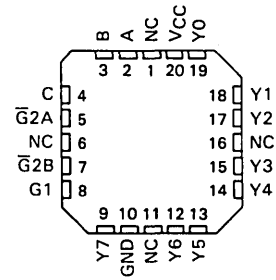
D2684, DECEMBER 1982

- **Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems**
- **Incorporates 3 Enable Inputs to Simplify Cascading and/or Data Reception**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC138 . . . J PACKAGE
SN74HC138 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC138 . . . FH OR FK PACKAGE
SN74HC138 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

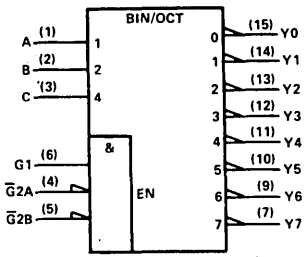
description

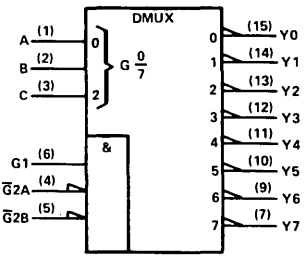
The 'HC138 circuit is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The conditions at the binary select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The SN54HC138 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC138 is characterized for operation from −40°C to 85°C.

logic symbols (alternatives)





Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table IV, page 2-6.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

FUNCTION TABLE

ENABLE INPUTS		SELECT INPUTS			OUTPUTS							
G1	$\overline{G2}$*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*$\overline{G2} = \overline{G2A} + \overline{G2B}$

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF						UNIT
						T_A = 25°C			SN54HC138		SN74HC138	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A, B, C	Any Y											ns
t_{PHL}													
t_{PLH}	Enable	Any Y											ns
t_{PHL}													

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

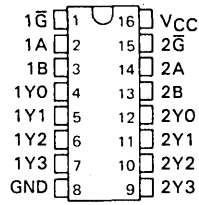
TYPES SN54HC139, SN74HC139
DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

D2684, DECEMBER 1982

- **Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems**
- **Incorporates 2 Enable Inputs to Simplify Cascading and/or Data Reception**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**

Dependable Texas Instruments Quality and Reliability

SN54HC139 . . . J PACKAGE
SN74HC139 . . . J OR N PACKAGE
(TOP VIEW)



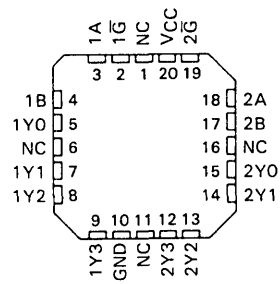
description

The 'HC139 circuit is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast-enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The 'HC139 is comprised of two individual two-line to four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications. These decoders/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit.

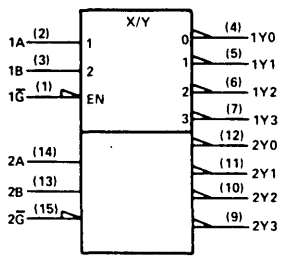
The SN54HC139 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC139 is characterized for operation from −40°C to 85°C.

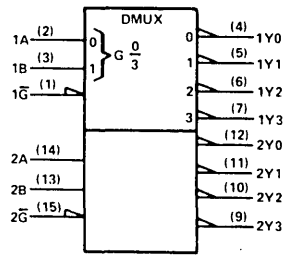
SN54HC139 . . . FH OR FK PACKAGE
SN74HC139 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

logic symbols (alternatives)





Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table IV, page 2-6.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

FUNCTION TABLE

INPUTS			OUTPUTS			
ENABLE	SELECT					
$\overline{G}$	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF				UNIT
						T_A = 25°C			SN54HC139	SN74HC139	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN MAX	MIN MAX	
t_{PLH}	A or B	Y									ns
t_{PHL}											
t_{PLH}	$\overline{G}$	Y									ns
t_{PHL}											

C_{pd}	*Power dissipation capacitance per decoder*	No load, T_A = 25°C	pF typ

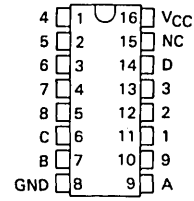
NOTE 1: For load circuit and voltage waveforms, see page 1-14.

TYPES SN54HC147, SN74HC147
10-LINE-TO-4-LINE PRIORITY ENCODERS

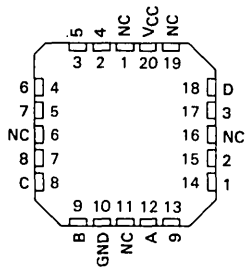
D2684, DECEMBER 1982

- Encodes 10-Line Decimal to 4-Line BCD
- Applications Include:
  Keyboard Encoding
  Range Selection
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54HC147 . . . J PACKAGE
SN74HC147 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC147 . . . FH OR FK PACKAGE
SN74HC147 . . . FH OR FN PACKAGE
(TOP VIEW)



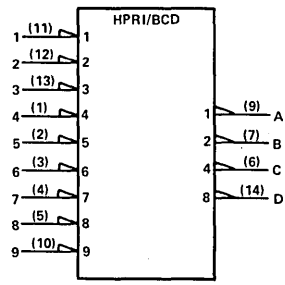
NC — No internal connection

description

These encoders feature priority decoding of the inputs to ensure that only the highest-order data line is encoded. The 'HC147 encodes nine data lines to four-line (8-4-2-1) BCD. The implied decimal zero condition requires no input condition as zero is encoded when all nine data lines are at a high logic level. The data inputs and outputs are active at the low logic level.

The SN54HC147 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC147 is characterized for operation from −40°C to 85°C.

logic symbol



Pin numbers shown are for J and N packages.

FUNCTION TABLE

INPUTS									OUTPUTS			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

maximum ratings, recommended operating conditions, and electrical characteristics

See Table IV, page 2-6.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF				UNIT
						T_A = 25°C		SN54HC147	SN74HC147	
			MIN	TYP	MAX	MIN	TYP MAX	MIN MAX	MIN MAX	
t_{PLH}	Any	Any (in phase with input)								ns
t_{PHL}										
t_{PLH}	Any	Any (out of phase with input)								ns
t_{PHL}										

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

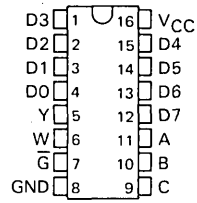
3

TYPES SN54HC151, SN74HC151
DATA SELECTORS/MULTIPLEXERS

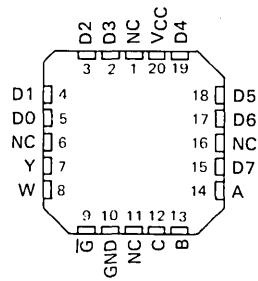
D2684, DECEMBER 1982

- **3-Line to 1-Line Multiplexers Can Perform As:**
  - **Boolean Function Generators**
  - **Parallel-to-Serial Converters**
  - **Data Source Selectors**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC151 . . . J PACKAGE
SN74HC151 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC151 . . . FH OR FK PACKAGE
SN74HC151 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

These monolithic data selectors/multiplexers provide full binary decoding to select one of eight data sources. The strobe input ($\overline{G}$) must be at a low logic level to enable the inputs. A high level at the strobe terminal forces the W output high and the Y output low.

The SN54HC151 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC151 is characterized for operation from −40°C to 85°C.

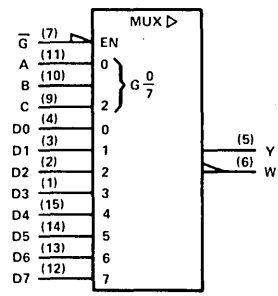
3

FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE	Y	W
C	B	A	$\overline{G}$		
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high level, L = low level, X = irrelevant
D0, D1 . . . D7 = the level of the D respective input

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table III, page 2-5.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, See Note 1				UNIT
						T_A = 25°C		SN54HC151	SN74HC151	
			MIN	TYP	MAX	MIN	TYP MAX	MIN MAX	MIN MAX	
t_{PLH}	A, B, or C	Y								ns
t_{PHL}										
t_{PLH}	A, B, or C	W								ns
t_{PHL}										
t_{PLH}	Any D	Y								ns
t_{PHL}										
t_{PLH}	Any D	W								ns
t_{PHL}										
t_{PLH}	$\overline{G}$	Y								ns
t_{PHL}										
t_{PLH}	$\overline{G}$	W								ns
t_{PHL}										

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

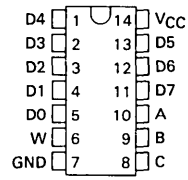
3

TYPES SN54HC152, SN74HC152
8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

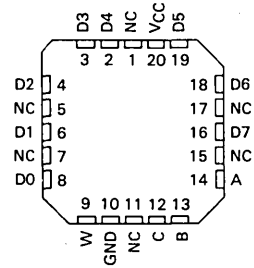
D2684, DECEMBER 1982

- Selects One-of-Eight Data Sources
- Performs Parallel-to-Serial Conversion
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54HC152 . . . J PACKAGE
SN74HC152 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC152 . . . FH OR FK PACKAGE
SN74HC152 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

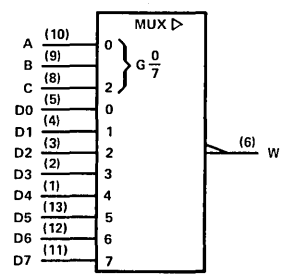
These monolithic data selectors/multiplexers contain full on-chip binary decoding to select the desired one-of-eight data sources.

The SN54HC152 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC152 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

SELECT INPUTS			OUTPUT
C	B	A	W
L	L	L	$\overline{D0}$
L	L	H	$\overline{D1}$
L	H	L	$\overline{D2}$
L	H	H	$\overline{D3}$
H	L	L	$\overline{D4}$
H	L	H	$\overline{D5}$
H	H	L	$\overline{D6}$
H	H	H	$\overline{D7}$

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table III, page 2-5.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, See Note 1				UNIT
						T_A = 25°C		SN54HC152	SN74HC152	
			MIN	TYP	MAX	MIN	TYP MAX	MIN MAX	MIN MAX	
t_{PLH}	A, B, or C	W								ns
t_{PHL}										
t_{PLH}	Any D	W								ns
t_{PHL}										

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

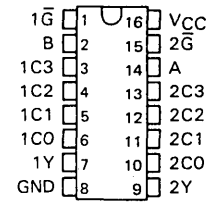
3

TYPES SN54HC153, SN74HC153
DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

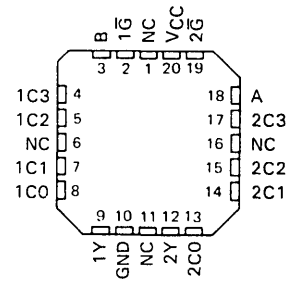
D2684, DECEMBER 1982

- Permits Multiplexing from N Lines to 1 Line
- Performs Parallel-to-Serial Conversion
- Strobe (Enable) Line Provided for Cascading (N lines to n lines)
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54HC153 . . . J PACKAGE
SN74HC153 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC153 . . . FH OR FK PACKAGE
SN74HC153 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate strobe inputs ($\overline{G}$) are provided for each of the two four-line sections.

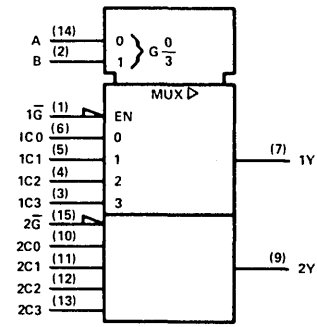
The SN54HC153 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC153 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table III, page 2-5.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, See Note 1				UNIT
						T_A = 25°C			SN54HC153	SN74HC153	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN MAX	MIN MAX	
t_{PLH}	A or B	Y									ns
t_{PHL}											
t_{PLH}	Data (Any C)	Y									ns
t_{PHL}											
t_{PLH}	G	Y									ns
t_{PHL}											

C_{pd}	Power dissipation capacitance per multiplexer	No load, T_A = 25°C	pF typ

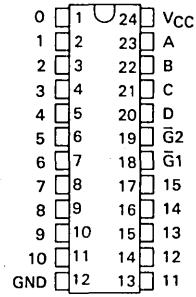
NOTE 1: For load circuit and voltage waveforms, see page 1-14.

TYPES SN54HC154, SN74HC154
4-LINE-TO-16-LINE DECODERS/DEMULTIPLEXERS

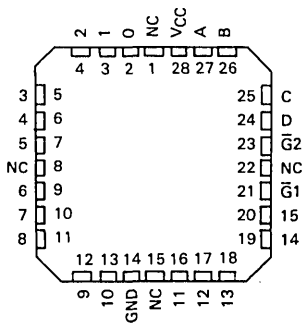
D2684, DECEMBER 1982

- **Decodes 4 Binary-Coded Inputs into One of 16 Mutually Exclusive Outputs**
- **Performs the Demultiplexing Function by Distributing Data From One Input Line to Any One of 16 Outputs**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC154 . . . JT PACKAGE
SN74HC154 . . . JT OR NT PACKAGE
(TOP VIEW)



SN54HC154 . . . FH OR FK PACKAGE
SN74HC154 . . . FH OR FN PACKAGE
(TOP VIEW)



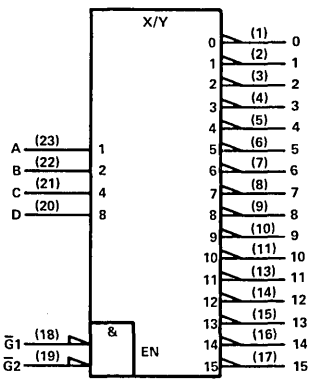
NC — No internal connection

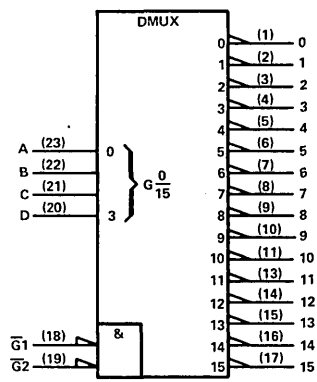
description

Each of these monolithic, 4-line-to-16-line decoders decodes four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs, $\overline{G}1$ and $\overline{G}2$, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. These demultiplexers are ideally suited for implementing high-performance memory decoders.

The SN54HC154 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC154 is characterized for operation from −40°C to 85°C.

logic symbols (alternatives)





Pin numbers shown are for JT and NT packages.

PRODUCT PREVIEW

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TEXAS INSTRUMENTS
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FUNCTION TABLE

OUTPUTS						OUTPUTS														
$\overline{G1}$	$\overline{G2}$	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high level, L = low level, X = irrelevant

3

maximum ratings, recommended operating conditions, and electrical characteristics

See Table IV, page 2-6.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF						UNIT
						T_A = 25°C			SN54HC154		SN74HC154	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A, B, C, or D	Any											ns
t_{PHL}													
t_{PLH}	$\overline{G1}$ or $\overline{G2}$	Any											ns
t_{PHL}													

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	pF typ

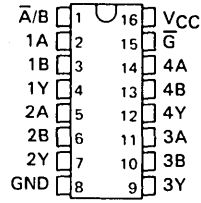
NOTE 1: For load circuit and voltage waveforms, see page 1-14.

TYPES SN54HC157, SN54HC158, SN74HC157, SN74HC158 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

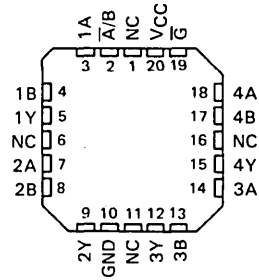
D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC157, SN54HC158 . . . J PACKAGE
SN74HC157, SN74HC158 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC157, SN54HC158 . . . FH OR FK PACKAGE
SN74HC157, SN74HC158 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

These monolithic data selectors/multiplexers contain inverters and drivers to supply full data selection to the four output gates. A separate strobe input ($\overline{G}$) is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The 'HC157 presents true data whereas the 'HC158 presents inverted data.

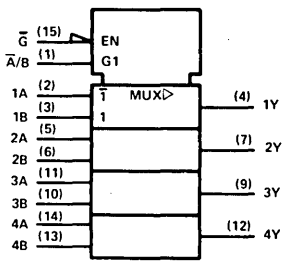
The SN54HC157 and SN54HC158 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC157 and SN74HC158 are characterized for operation from −40°C to 85°C.

FUNCTION TABLE

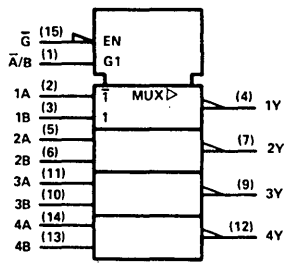
INPUTS				OUTPUT Y	
STROBE $\overline{G}$	SELECT $\overline{A}$/B	DATA A	DATA B	'HC157	'HC158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

logic symbols

'HC157



'HC158



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table III, page 2-5.

PRODUCT PREVIEW

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'HC157 switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, See Note 1			UNIT
				T_A = 25°C	SN54HC157	SN74HC157	
			MIN TYP MAX	MIN TYP MAX	MIN MAX	MIN MAX	
t_{PLH}	A or B	Y					ns
t_{PHL}							
t_{PLH}	$\overline{A}$/B	Y					ns
t_{PHL}							
t_{PLH}	$\overline{G}$	Y					ns
t_{PHL}							

C_{pd}	Power dissipation capacitance per multiplexer	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

3

'HC158 switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, See Note 1			UNIT
				T_A = 25°C	SN54HC158	SN74HC158	
			MIN TYP MAX	MIN TYP MAX	MIN MAX	MIN MAX	
t_{PLH}	A or B	Y					ns
t_{PHL}							
t_{PLH}	$\overline{A}$/B	Y					ns
t_{PHL}							
t_{PLH}	$\overline{G}$	Y					ns
t_{PHL}							

C_{pd}	Power dissipation capacitance per multiplexer	No load, T_A = 25°C	pF typ

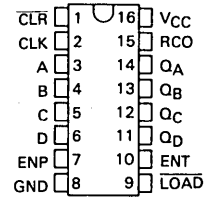
NOTE 1: For load circuit and voltage waveforms, see page 1-14.

TYPES SN54HC160 THRU SN54HC163, SN74HC160 THRU SN74HC163
SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS

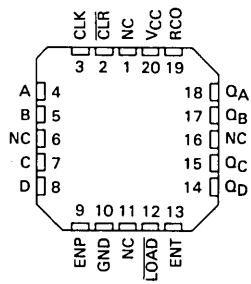
D2684, DECEMBER 1982

- **Internal Look-Ahead for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Synchronous Counting**
- **Synchronously Programmable**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC'. . . J PACKAGE
SN74HC'. . . J or N PACKAGE
(TOP VIEW)



SN54HC' . . . FH or FK PACKAGE
SN74HC' . . . FH or FN PACKAGE
(TOP VIEW)



NC — no internal connection

description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The 'HC160 and 'HC162 are decade counters, and the 'HC161 and 'HC163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with synchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs.

The clear function for the 'HC160 and 'HC161 is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of the clock, load, or enable inputs.

The clear function for the 'HC162 and 'HC163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (ENP and ENT) must be high to count, and ENT is fed forward to enable the ripple carry output. The ripple carry output (RCO) thus enabled will produce a high-level pulse while the count is maximum (9 or 15 with Q_A high). This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the ENP or ENT are allowed regardless of the level of the clock input.

These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or $\overline{\text{LOAD}}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

The SN54HC160 through SN54HC163 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC160 through SN74HC163 are characterized for operation from −40°C to 85°C.

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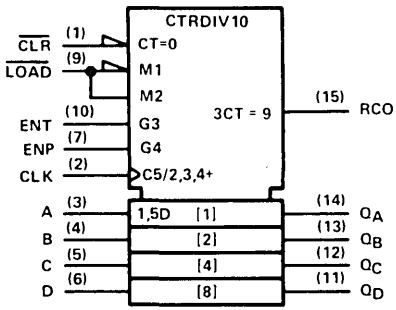
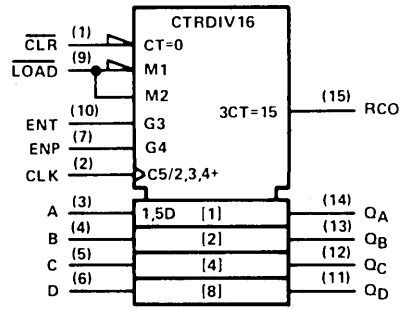
logic symbols

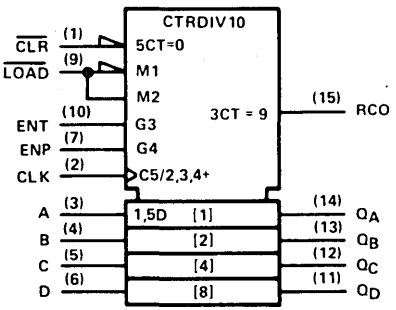
HC160 DECADE COUNTER
WITH DIRECT CLEAR



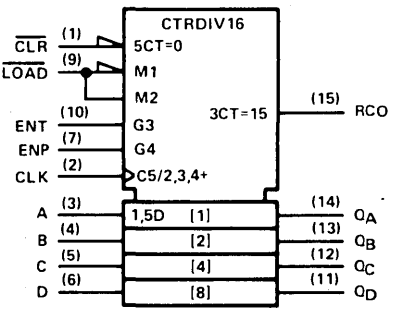
'HC161 BINARY COUNTER
WITH DIRECT CLEAR



'HC162 DECADE COUNTER
WITH SYNCHRONOUS CLEAR



'HC163 BINARY COUNTER
WITH SYNCHRONOUS CLEAR

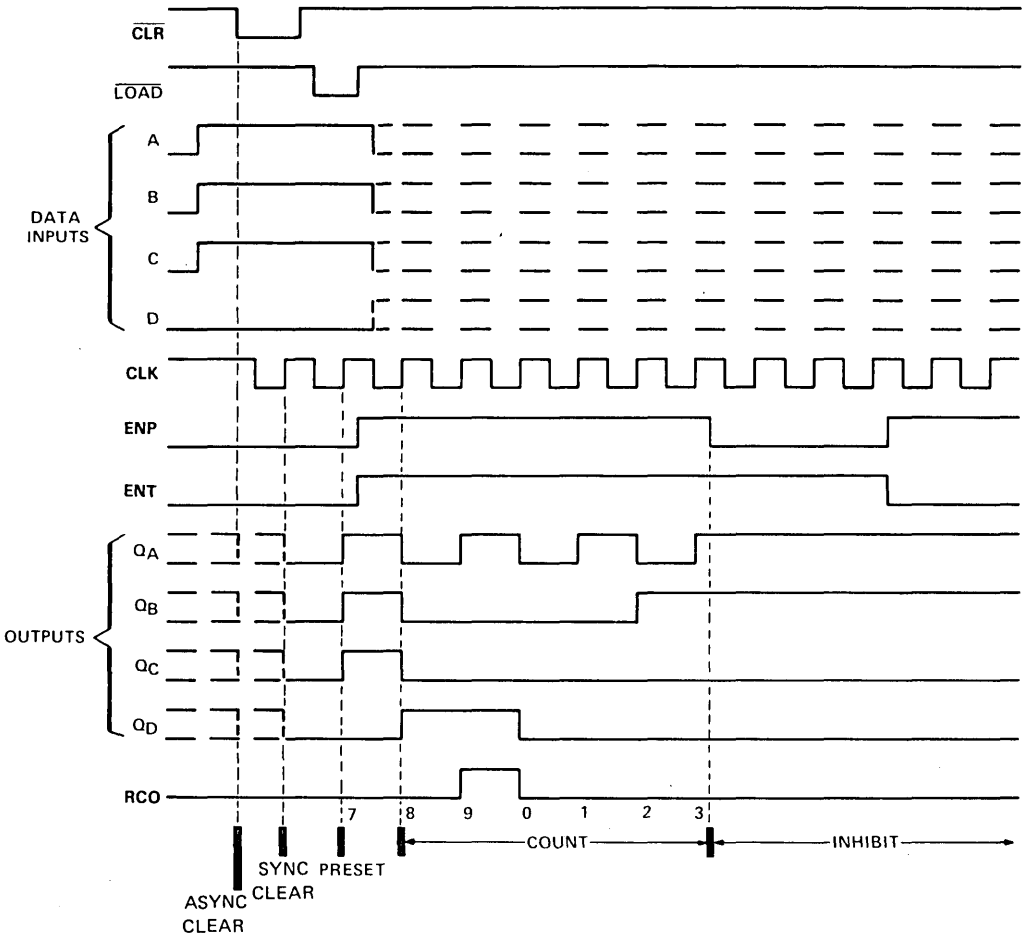


Pin numbers shown are for J and N packages.

'160 and '162 output sequence

Illustrated below is the following sequence:

1. Clear outputs to zero (SN54HC160 and SN74HC160 are asynchronous; SN54HC162 and SN74HC162 are synchronous)
2. Preset to BCD seven
3. Count to eight, nine, zero, one, two, and three
4. Inhibit



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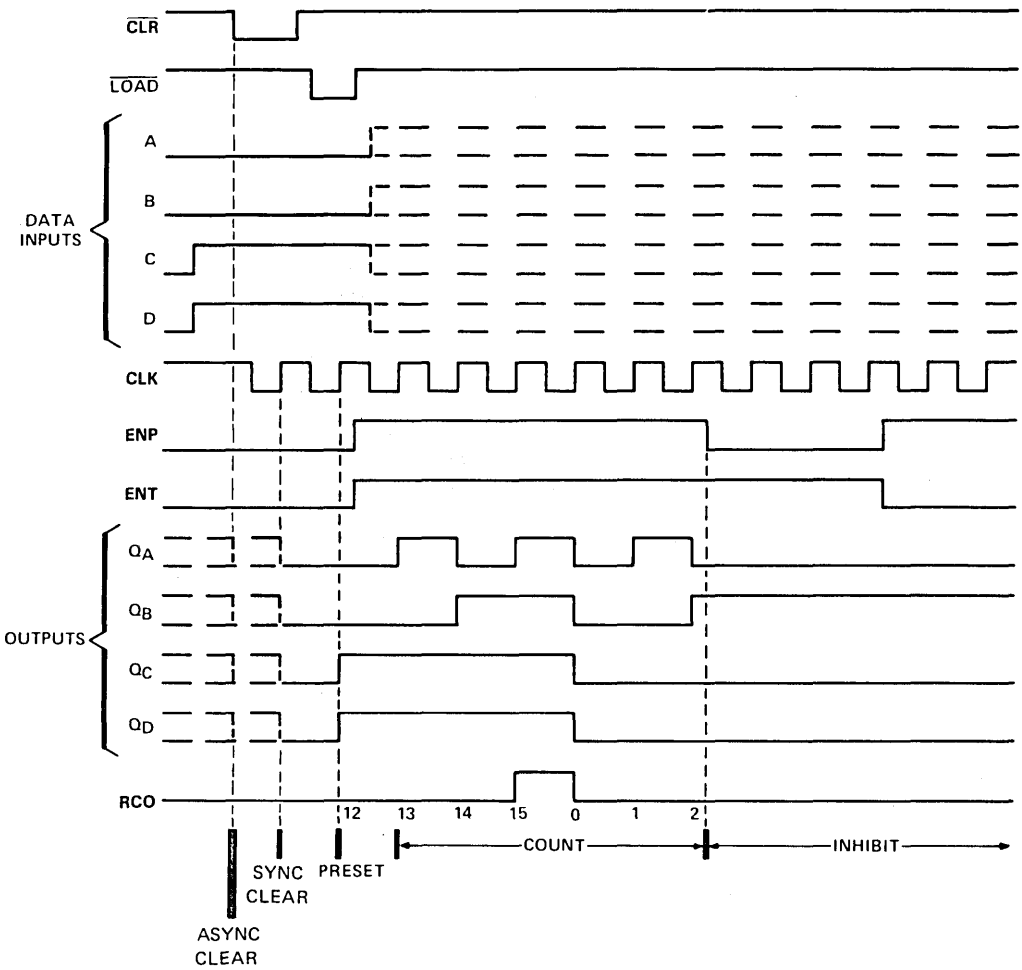
'161 and '163 output sequence

Illustrated below is the following sequence:

1. Clear outputs to zero (SN54HC161 and SN74HC161 are asynchronous; SN54HC163 and SN74HC163 are synchronous)
2. Preset to binary twelve
3. Count to thirteen, fourteen, zero, one, and two
4. Inhibit



maximum ratings, recommended operating conditions, and electrcical characteristics

See Table IV, page 2-6.

timing requirements (supplement to recommended operating conditions)

				SN54HC160 THRU SN54HC163			SN74HC160 THRU SN74HC163			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}	Clock frequency									MHz
t_w	Pulse duration	CLK high or low	'HC160, 'HC162							ns
			'HC161, 'HC163							
		'HC160, 'HC161	$\overline{CLR}$ low							
t_{su}	Setup time before CLK↑	A, B, C, D								ns
		ENP, ENT	'HC160, 'HC161							
			'HC162, 'HC163							
		'HC160, 'HC161	$\overline{CLR}$ inactive							
		'HC162, 'HC163	$\overline{CLR}$ low							
			$\overline{CLR}$ high (inactive)							
t_h	Hold time, all synchronous inputs after CLK↑									ns

3

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF						UNIT
						T_A = 25°C			SN54HC'		SN74HC'	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	MIN	MAX
f_{max}												MHz
t_{PLH}	CLK	RCO										ns
t_{PHL}												
t_{PLH}	CLK	Any Q										ns
t_{PHL}												
t_{PLH}	ENT	RCO										ns
t_{PHL}												
t_{PHL}	$\overline{CLR}$	Any Q										ns
t_{PHL}	$\overline{CLR}$	RCO										ns

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

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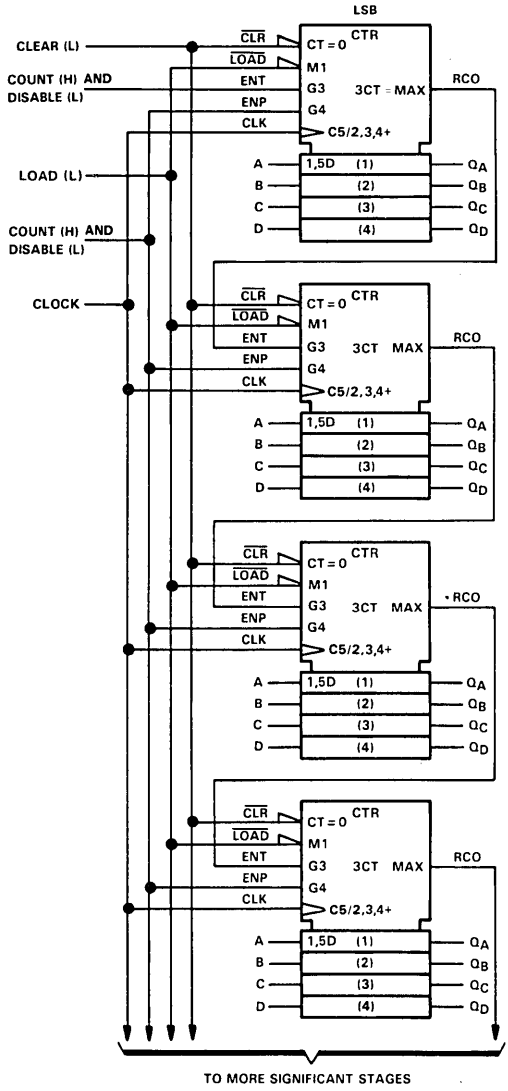
TYPICAL APPLICATION DATA

N-BIT SYNCHRONOUS COUNTERS

This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter. The 'HC160 and 'HC162 will count in BCD, and the 'HC161 and 'HC163 will count in binary. Virtually any count mode (modulo-N, N_1-to-N_2, N_1-to-maximum) can be used with this fast look-ahead circuit.

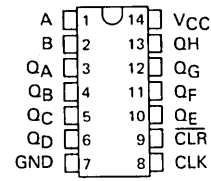


TYPES SN54HC164, SN74HC164 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

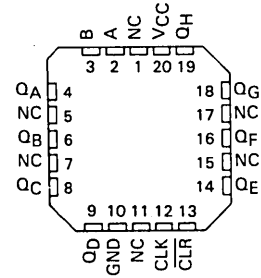
D2684, DECEMBER 1982

- AND-Gated (Enable/Disable) Serial Inputs
- Fully Buffered Clock and Serial Inputs
- Direct Clear
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54HC164 . . . J PACKAGE
SN74HC164 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC164 . . . FH OR FK PACKAGE
SN74HC164 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

These 8-bit shift registers feature AND-gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input, which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of the clock input.

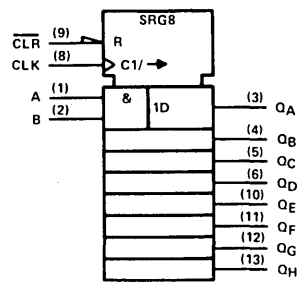
The SN54HC164 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74HC164 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

INPUTS				OUTPUTS		
CLEAR	CLOCK	A	B	Q_A	Q_B . . . Q_H	
L	X	X	X	L	L	L
H	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	↑	H	H	H	Q_{An}	Q_{Gn}
H	↑	L	X	L	Q_{An}	Q_{Gn}
H	↑	X	L	L	Q_{An}	Q_{Gn}

H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level.
Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most-recent ↑ transition of the clock; indicates a one-bit shift.

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table IV, page 2-6.

PRODUCT PREVIEW

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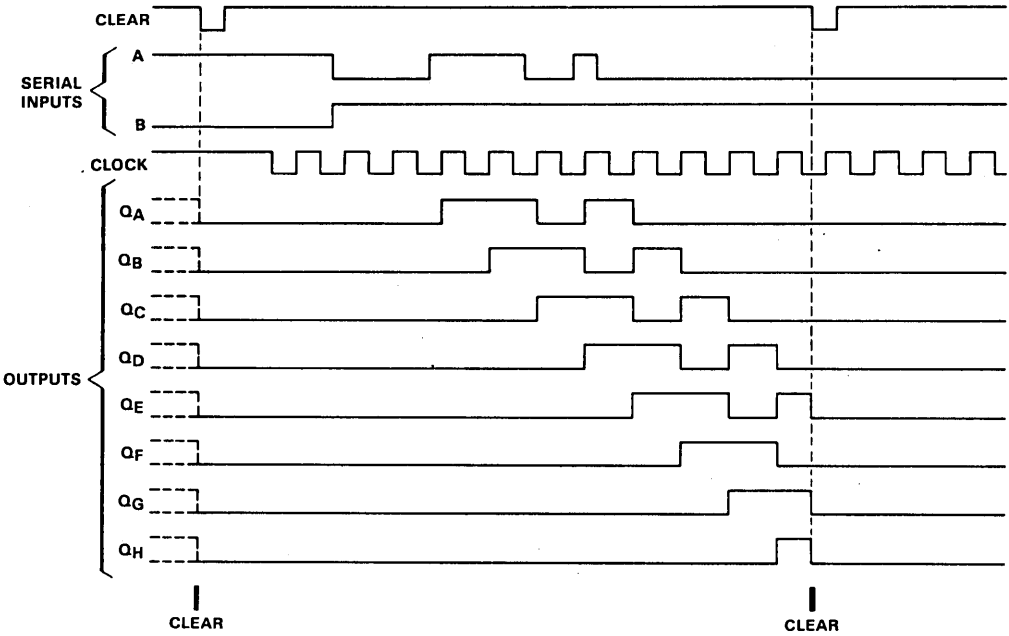
typical clear, shift, and clear sequences



timing requirements (supplement to recommended operating conditions)

			SN54HC164			SN74HC164			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	$\overline{CLR}$ low							ns
		CLK high							
		CLK low							
t_{su}	Setup time before CLK↑	Data							ns
		$\overline{CLR}$ inactive							
t_h	Hold time, data after CLK↑								ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF					UNIT
						T_A = 25°C			SN54HC164	SN74HC164	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN MAX	MIN MAX	
f_{max}											MHz
t_{PHL}	$\overline{CLR}$	Any Q									ns
t_{PLH}	CLK	Any Q									ns
t_{PHL}											

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	pF typ

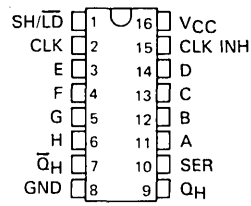
NOTE 1: For load circuit and voltage waveforms, see page 1-14.

TYPES SN54HC165, SN74HC165
PARALLEL-LOAD 8-BIT SHIFT REGISTERS

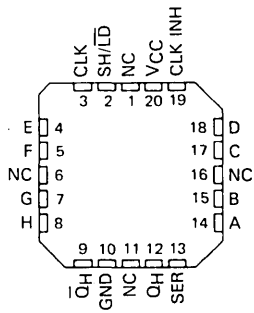
D2684, DECEMBER 1982

- **Complementary Outputs**
- **Direct Overriding Load (Data) Inputs**
- **Gated Clock Inputs**
- **Parallel-to-Serial Data Conversion**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC165 . . . J PACKAGE
SN74HC165 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC165 . . . FH OR FK PACKAGE
SN74HC165 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

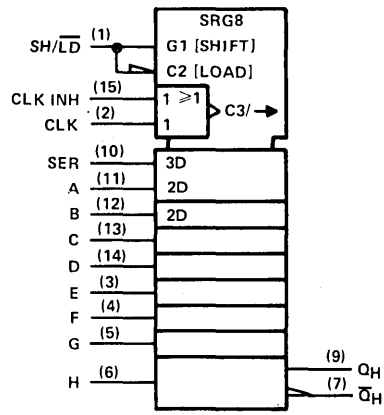
description

The 'HC165 is an 8-bit serial shift register that, when clocked, shifts the data toward serial output Q_H. Parallel-in access to each stage is provided by eight individual direct data inputs that are enabled by a low level at the SH/$\overline{LD}$ input. The 'HC165 also features a clock inhibit function and a complementary serial output Q_H.

Clocking is accomplished by a low-to-high transition of the CLK input while SH/$\overline{LD}$ is held high and CLK INH is held low. The functions of the CLK and CLK INH (clock inhibit) inputs are interchangeable. Since a low CLK input and a low-to-high transition of CLK INH will also accomplish clocking, CLK INH should be changed to the high level only while the CLK input is high. Parallel loading is inhibited when SH/$\overline{LD}$ is held high. The parallel inputs to the register are enabled while SH/$\overline{LD}$ is low independently of the levels of CLK, CLK INH, or SER inputs.

The SN54HC165 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC165 is characterized for operation from −40°C to 85°C.

logic symbol



Pin numbers shown are for J and N packages.

FUNCTION TABLE

INPUTS			FUNCTION
SH/$\overline{LD}$	CLK	CLK INH	
L	X	X	PARALLEL LOAD
H	H	X	NO CHANGE
H	X	H	NO CHANGE
H	L	↑	SHIFT
H	↑	L	SHIFT

SHIFT – content of each internal register shifts toward serial output Q_H. Data at serial input is shifted into first register.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table IV, page 2-6.

TEXAS INSTRUMENTS
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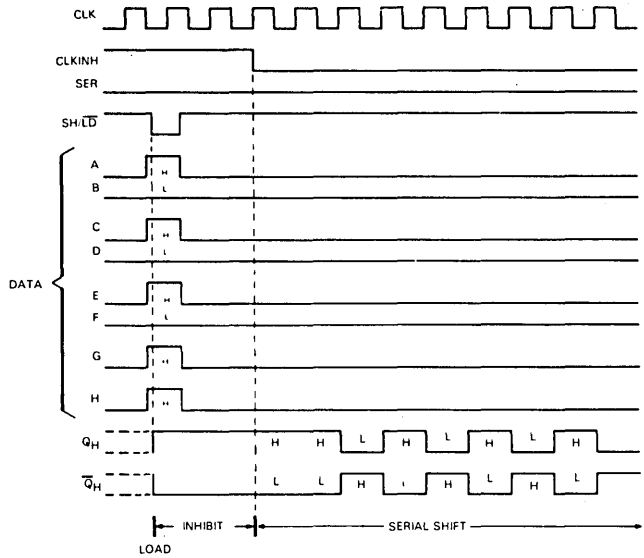
typical shift, load, and inhibit sequences



timing requirements (supplement to recommended operating conditions)

			SN54HC165			SN74HC165			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	SH/$\overline{LD}$ low							ns
		CLK high							
		CLK low							
t_{su}	Setup time	SH/$\overline{LD}$ high before CLK↑							ns
		SER before CLK↑							
		CLK INH before CLK↑							
		Data before SH/$\overline{LD}$↑							
t_h	Hold time, SER after CLK↑								ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF						UNIT
						T_A = 25°C			SN54HC165		SN74HC165	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}													MHz
t_{PLH}	SH/$\overline{LD}$	Q_H											ns
t_{PHL}													
t_{PLH}		$\overline{Q}_H$											
t_{PHL}													
t_{PLH}	CLK	Q_H											ns
t_{PHL}													
t_{PLH}		$\overline{Q}_H$											
t_{PHL}													
t_{PLH}	H	Q_H											ns
t_{PHL}													
t_{PLH}		$\overline{Q}_H$											
t_{PHL}													

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

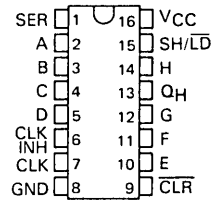
3

TYPES SN54HC166, SN74HC166
PARALLEL-LOAD 8-BIT SHIFT REGISTERS

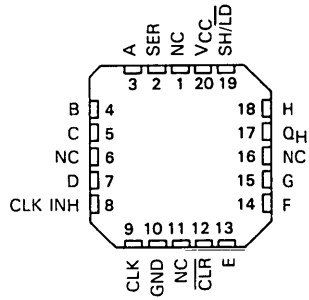
D2684, DECEMBER 1982

- **Synchronous Load**
- **Direct Overriding Clear**
- **Parallel to Serial Conversion**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC166 . . . J PACKAGE
SN74HC166 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC166 . . . FH OR FK PACKAGE
SN74HC166 . . . FH OR FN PACKAGE
(TOP VIEW)



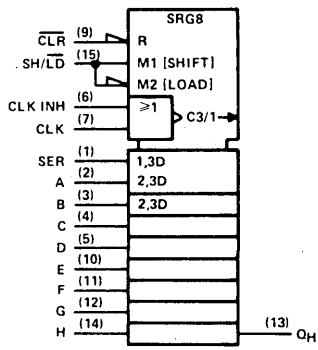
NC — No internal connection

description

The 'HC166 parallel-in or serial-in, serial-out registers feature gated clock inputs and an overriding clear input. The parallel-in or serial-in modes are established by the shift/load input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input positive NOR gate permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This, of course, allows the system clock to be free-running and the register can be stopped on command with the clock input. The clock-inhibit input should be changed to the high level only when the clock input is high. A direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

The SN54HC166 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC166 is characterized for operation from −40°C to 85°C.

logic symbol



Pin numbers shown are for J and N packages.

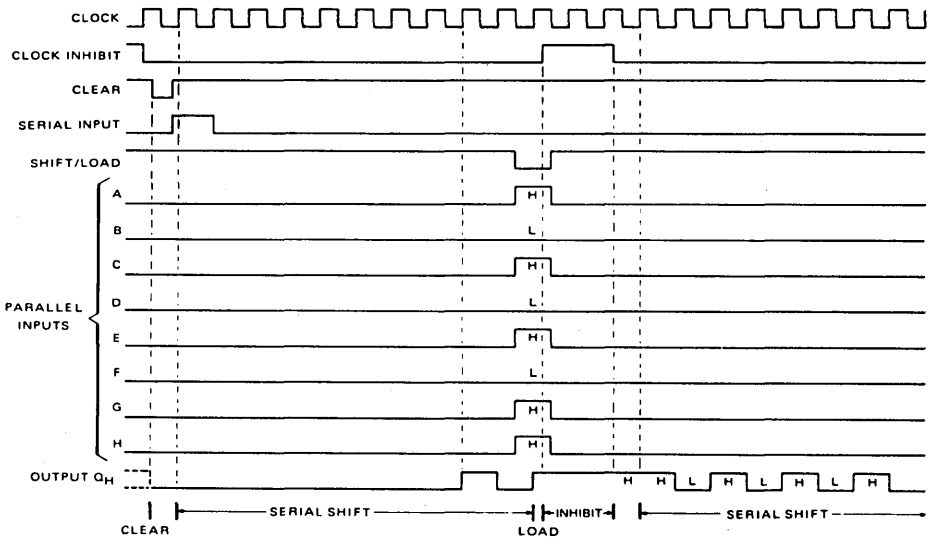
FUNCTION TABLE

INPUTS						INTERNAL OUTPUTS		OUTPUT
CLEAR	SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A . . . H	Q_A	Q_B	Q_H
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a . . . h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

maximum ratings, recommended operating conditions, and electrical characteristics

See Table IV, page 2-6.

typical clear, shift, load, inhibit, and shift sequences



timing requirements (supplement to recommended operating conditions)

			SN54HC166			SN74HC166			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	$\overline{CLR}$ low							ns
		SH/$\overline{LD}$ low							
		CLK high							
		CLK low							
t_{su}	Setup time before CLK↑	SH/$\overline{LD}$ high before CLK↑							ns
		SER before CLK↑							
		CLK INH before CLK↑							
		Data before SH/$\overline{LD}$↑							
		$\overline{CLR}$ inactive							
t_h	Hold time, SER after CLK↑								ns

TEXAS INSTRUMENTS
INCORPORATED
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switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF						UNIT
						T_A = 25°C			SN54HC166		SN74HC166	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}													MHz
t_{PHL}	$\overline{CLR}$	Q_H											ns
t_{PLH}	CLK	Q_H											ns
t_{PHL}													
t_{PLH}	SH/$\overline{LD}$	Q_H											ns
t_{PHL}													
t_{PLH}	H	Q_H											ns
t_{PHL}													

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

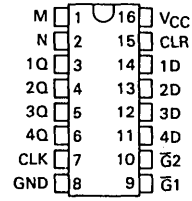
3

TYPES SN54HC173, SN74HC173
4-BIT D-TYPE REGISTERS WITH 3-STATE OUTPUTS

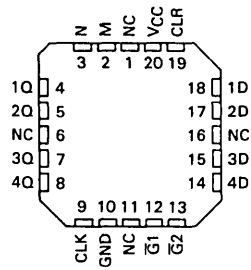
D2684, DECEMBER 1982

- **High-Current 3-State Outputs Interface Directly with System Bus or Can Drive up to 15 LSTTL Loads**
- **Gated Output-Control Lines for Enabling or Disabling the Outputs**
- **Fully Independent Clock Virtually Eliminates Restrictions for Operating in One of Two Modes**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC173 . . . J PACKAGE
SN74HC173 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC173 . . . FH OR FK PACKAGE
SN74HC173 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

The 'HC173 four-bit registers include D-type flip-flops featuring totem-pole three-state outputs capable of driving highly capacitive or relatively low-impendance loads. The high-impedance third state and increased drive provide these flip-flops with the capability of being connected directly to and driving the lines in a bus-organized system without need for interface or pull-up components.

Gated enable inputs are provided on these devices for controlling the entry of data into the flip-flops. When both data-enable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the clock input. Gate output control inputs are also provided. When both are low, the normal logic states (high or low levels) of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at either output control input. The outputs then present a high impedance and neither load nor drive the bus line. Detailed operation is given in the function table.

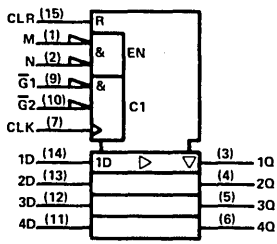
The SN54HC173 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74HC173 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

INPUTS					OUTPUT
CLEAR	CLOCK	DATA ENABLE $\overline{G1}$	DATA ENABLE $\overline{G2}$	DATA D	Q
H	X	X	X	X	L
L	L	X	X	X	Q_0
L	↑	H	X	X	Q_0
L	↑	X	H	X	Q_0
L	↑	L	L	L	L
L	↑	L	L	H	H

When either M or N (or both) is (are) high the output is disabled to the high-impedance state; however sequential operation of the flip-flops is not affected.

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table III, page 2-5.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
INCORPORATED
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timing requirements (supplement to recommended operating conditions)

			SN54HC173			SN74HC173			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}	Input clock frequency								MHz
t_w	Pulse duration	CLK high or low							ns
		CLR low							
t_{su}	Setup time before CLK↑	$\overline{G}1$ and $\overline{G}2$ low							ns
		Data							
		CLR inactive							
t_h	Hold time after CLK↑	$\overline{G}1$ and $\overline{G}2$ low							ns
		Data							

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 45 pF, R_L = 667Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, See Note 1					UNIT
						T_A = 25°C			SN54HC173	SN74HC173	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN MAX	MIN MAX	
f_{max}											MHz
t_{PHL}	CLR	Any									ns
t_{PLH}	CLK	Any									ns
t_{PHL}											
t_{PZH}	M or N	Any									ns
t_{PZL}											
t_{PHZ}	M or N	Any									ns
t_{PLZ}											

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

3

TYPES SN54HC174, SN54HC175, SN74HC174, SN74HC175 HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

D2684, DECEMBER 1982

- 'HC174 Contains Six Flip-Flops with Single-Rail Outputs
- 'HC175 Contains Four Flip-Flops with Double-Rail Outputs
- Applications Include:
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These monolithic, positive-edge-triggered D-type flip-flops have a direct clear input and the 'HC175 features complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going edge of the clock pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

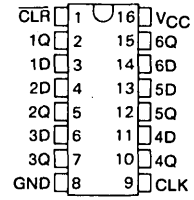
The SN54HC174 and SN54HC175 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC174 and SN74HC175 are characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(EACH FLIP-FLOP)

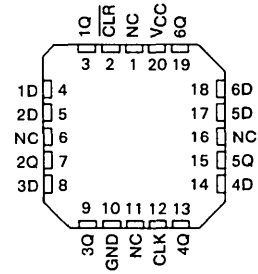
INPUTS			OUTPUTS	
$\overline{CLR}$	CLK	D	Q	$\overline{Q}$†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

†'HC175 only

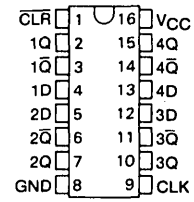
SN54HC174 . . . J PACKAGE
SN74HC174 . . . J OR N PACKAGE
(TOP VIEW)



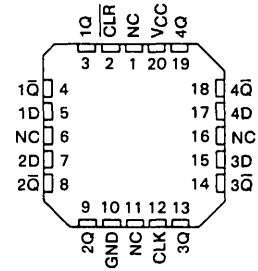
SN54HC174 . . . FH OR FK PACKAGE
SN74HC174 . . . FH OR FN PACKAGE
(TOP VIEW)



SN54HC175 . . . J PACKAGE
SN74HC175 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC175 . . . FH OR FK PACKAGE
SN74HC175 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

TEXAS INSTRUMENTS
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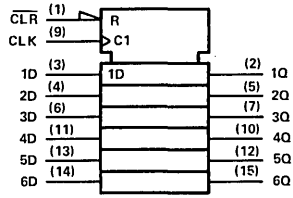
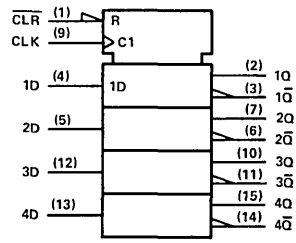
logic symbols

'HC174



'HC175



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

'HC174 See Table IV, page 2-6.
'HC175 See Table II, page 2-4.

timing requirements (supplement to recommended operating conditions)

			SN54HC174 SN54HC175			SN74HC174 SN74HC175			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	$\overline{CLR}$ low							ns
		CLK high							
		CLK low							
t_{su}	Setup time before CLK↑	Data							ns
		$\overline{CLR}$ inactive							
t_h	Hold time, data after CLK↑								ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF					UNIT
						T_A = 25°C			SN54HC174 SN54HC175	SN74HC174 SN74HC175	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN MAX	MIN MAX	
f_{max}											MHz
t_{PLH}	$\overline{CLR}$	Any $\overline{Q}$ ('HC175)									ns
t_{PHL}		Any Q									
t_{PLH}	CLK	Any Q (or $\overline{Q}$, 'HC175)									ns
t_{PHL}											

C_{pd}	Power dissipation capacitance per flip-flop	No load, T_A = 25°C	pF typ

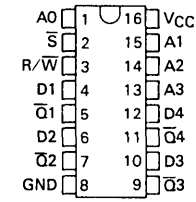
NOTE 1: For load circuit and voltage waveforms, see page 1-14.

TYPES SN54HC189, SN74HC189
64-BIT RANDOM-ACCESS MEMORIES

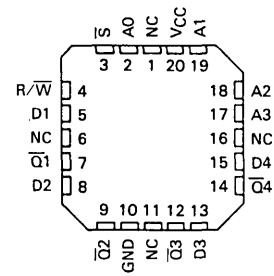
D2684, DECEMBER 1982

- **Organized as 16 Words of Four Bits Each**
- **High-Current 3-State Inverting Outputs Can Drive up to 15 LSTTL Loads**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC189 . . . J PACKAGE
SN74HC189 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC189 . . . FH OR FK PACKAGE
SN74HC189 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

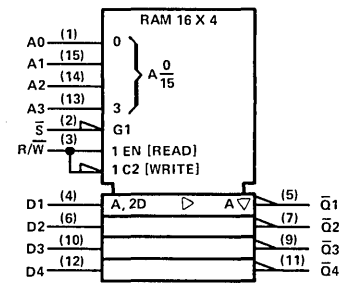
description

Information to be stored in the memory is written into the selected address location when the chip-select ($\overline{S}$) and the write-enable ($R/\overline{W}$) inputs are low. While the write-enable input is low, the memory outputs are off (Hi-Z). When a number of outputs are bus-connected, this off state neither loads nor drives the data bus; however, it permits the bus line to be driven by other active outputs or a passive pull-up.

Information stored in the memory (see function table for input/output phase relationship) is available at the outputs when the write-enable input is high and the chip-select input is low. When the chip-select input is high, the outputs will be off.

The SN54HC189 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC189 is characterized for operation from −40°C to 85°C.

logic symbol



Pin numbers shown are for J and N packages.

FUNCTION TABLE

FUNCTION	INPUTS		OUTPUTS
	CHIP SELECT	WRITE ENABLE	
Write	L	L	Z
Read	L	H	Complement of Data Entered
Inhibit	H	X	Z

maximum ratings, recommended operating conditions, and electrical characteristics

See Table III, page 2-5.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

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timing requirements (supplement to recommended operating conditions)

			SN54HC189			SN74HC189			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
t_w	Pulse duration, R/$\overline{W}$ low								ns
t_{su}	Setup time	Address before R/$\overline{W}$↓							ns
		Data before R/$\overline{W}$↑							
		Chip-select before R/$\overline{W}$↑							
t_h	Hold time	Address after R/$\overline{W}$↑							ns
		Data after R/$\overline{W}$↑							
		Chip-select after R/$\overline{W}$↑							

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 45 pF, R_L = 667Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, See Note 1					UNIT
						T_A = 25°C			SN54HC189	SN74HC189	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN MAX	MIN MAX	
$t_{a(ad)}$	A	Any									ns
$t_{a(S)}$	$\overline{S}$	Any									ns
t_{sr}											ns
t_{dis}	$\overline{S}$	Any									ns
	R/$\overline{W}$	Any									

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	*pF typ*

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

3

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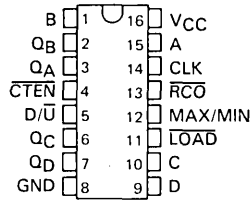
HIGH-SPEED CMOS LOGIC

TYPES SN54HC190, SN54HC191, SN74HC190, SN74HC191 SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS

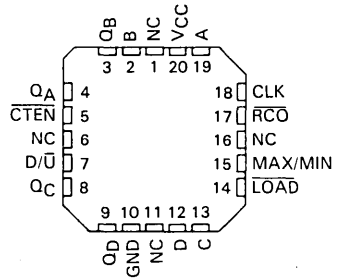
D2684, DECEMBER 1982

- **Single Down/Up Count Control Line**
- **Look-Ahead Circuitry Enhances Speed of Cascaded Counters**
- **Fully Synchronous in Count Modes**
- **Asynchronously Presettable with Load Control**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC190, SN54HC191 . . . J PACKAGE
SN74HC190, SN74HC191 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC190, SN54HC191 . . . FH OR FK PACKAGE
SN74HC190, SN74HC191 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

The 'HC190 and 'HC191 are synchronous, reversible up/down counters. The 'HC190 is a 4-bit decade counter and the 'HC191 is a 4-bit binary counter. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input ($\overline{CTEN}$) is low. A high at $\overline{CTEN}$ inhibits counting. The direction of the count is determined by the level of the down/up (D/$\overline{U}$) input. When D/$\overline{U}$ is low, the counter counts up and when D/$\overline{U}$ is high, it counts down.

These counters feature a fully independent clock circuit. Changes at the control inputs ($\overline{CTEN}$ and D/$\overline{U}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter will be dictated solely by the condition meeting the stable setup and hold times.

These counters are fully programmable; that is, the outputs may each be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

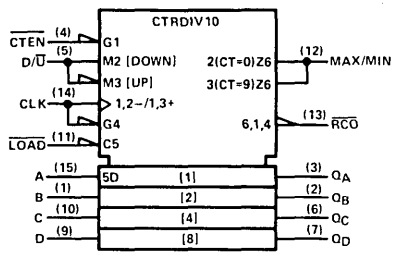
Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down or maximum (9 or 15) counting up. The ripple clock output produces a low-level output pulse under those same conditions but only while the clock input is low. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

The SN54HC190 and SN54HC191 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC190 and SN74HC191 are characterized for operation from −40°C to 85°C.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table IV, page 2-6.

'HC190 logic symbol

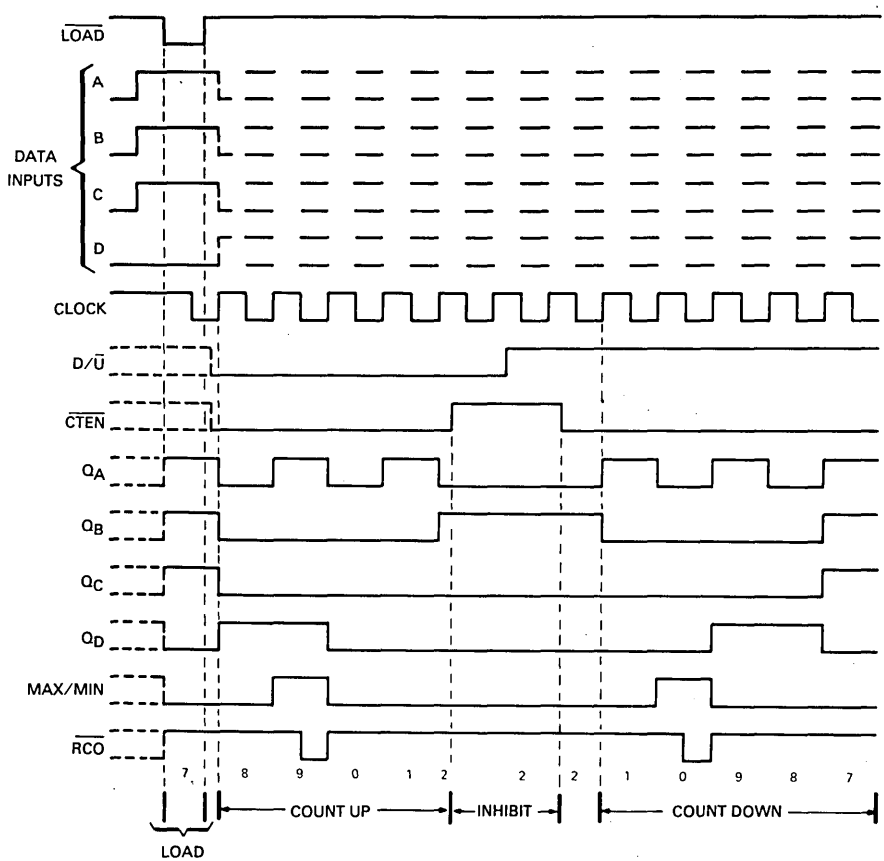


Pin numbers shown are for J and N packages.

typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to BCD seven.
2. Count up to eight, nine (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), nine, eight, and seven.



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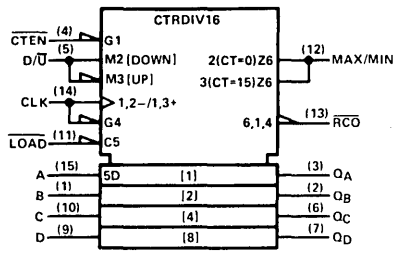
'HC191 logic symbol

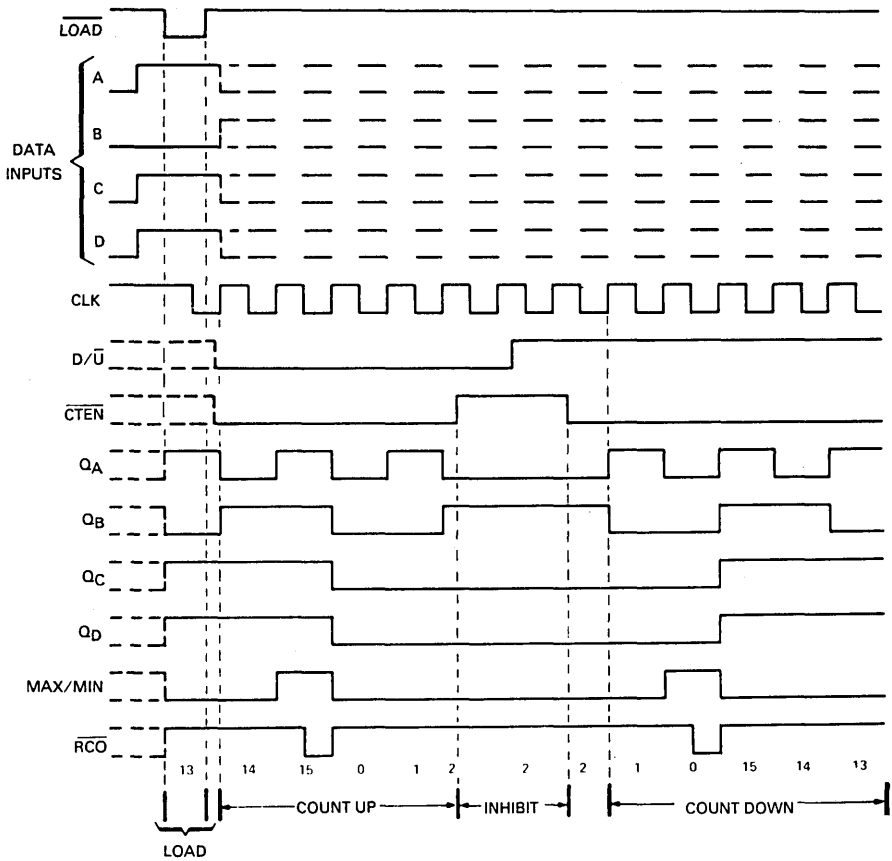


Pin numbers shown are for J and N packages.

typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen.
2. Count up to fourteen, fifteen (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.



timing requirements (supplement to recommended operating conditions)

			SN54HC190 SN54HC191			SN74HC190 SN74HC191			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}	Clock frequency	'HC190							MHz
		'HC191							
t_w	Pulse duration	CLK high							ns
		CLK low							
		$\overline{LOAD}$ low							
t_{su}	Setup time	Data before $\overline{LOAD}$↑							ns
		$\overline{CTEN}$ before CLK↑							
		D/$\overline{U}$ before CLK↑							
		$\overline{LOAD}$ inactive before CLK↑							
t_h	Hold time	Data after $\overline{LOAD}$↑							ns
		$\overline{CTEN}$ after CLK↑							
		D/$\overline{U}$ after CLK↑							

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF						UNIT
						T_A = 25°C			SN54HC190 SN54HC191		SN74HC190 SN74HC191	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	MIN	MAX
f_{max}	'HC190											MHz
	'HC191											
t_{PLH}	$\overline{LOAD}$	Any Q										ns
t_{PHL}												
t_{PLH}	A, B, C, D	Any Q										ns
t_{PHL}												
t_{PLH}	CLK	$\overline{RCO}$										ns
t_{PHL}												
t_{PLH}	CLK	Any Q										ns
t_{PHL}												
t_{PLH}	CLK	MAX/MIN										ns
t_{PHL}												
t_{PLH}	D/$\overline{U}$	$\overline{RCO}$										ns
t_{PHL}												
t_{PLH}	D/$\overline{U}$	MAX/MIN										ns
t_{PHL}												
t_{PLH}	$\overline{CTEN}$	$\overline{RCO}$										ns
t_{PHL}												

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

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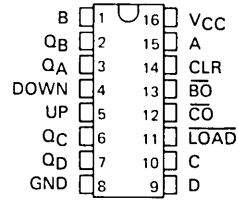
TYPES SN54HC192, SN54HC193, SN74HC192, SN74HC193 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

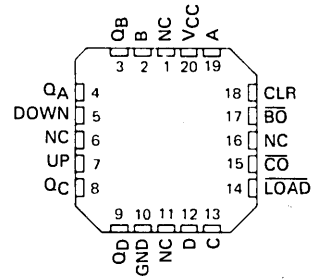
D2684, DECEMBER 1982

- **Look-Ahead Circuitry Enhances Cascaded Counters**
- **Fully Synchronous in Count Modes**
- **Parallel Asynchronous Load for Modulo-N Count Lengths**
- **Asynchronous Clear**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC192, SN54HC193 . . . J PACKAGE
SN74HC192, SN74HC193 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC192, SN54HC193 . . . FH OR FK PACKAGE
SN74HC192, SN74HC193 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

The 'HC192 and 'HC193 are synchronous, reversible up/down counters. The 'HC192 is a 4-bit decade counter and the 'HC193 is a 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered by a low-to-high-level transition of either count (clock) input (Up or Down). The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and the load inputs.

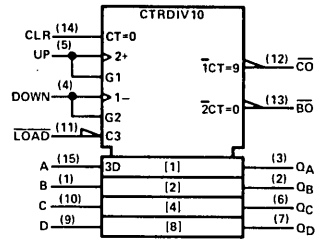
These counters were designed to be cascaded without the need for external circuitry. The borrow output ($\overline{BO}$) produces a low-level pulse while the count is zero (all outputs low) and the count-down is low. Similarly, the carry output ($\overline{CO}$) produces a low-level pulse while the count is maximum (9 or 15) and the count-up input is low. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs, respectively, of the succeeding counter.

The SN54HC192 and SN54HC193 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74HC192 and SN74HC193 are characterized for operation from -40°C to 85°C.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table IV, page 2-6.

'HC192 logic symbol

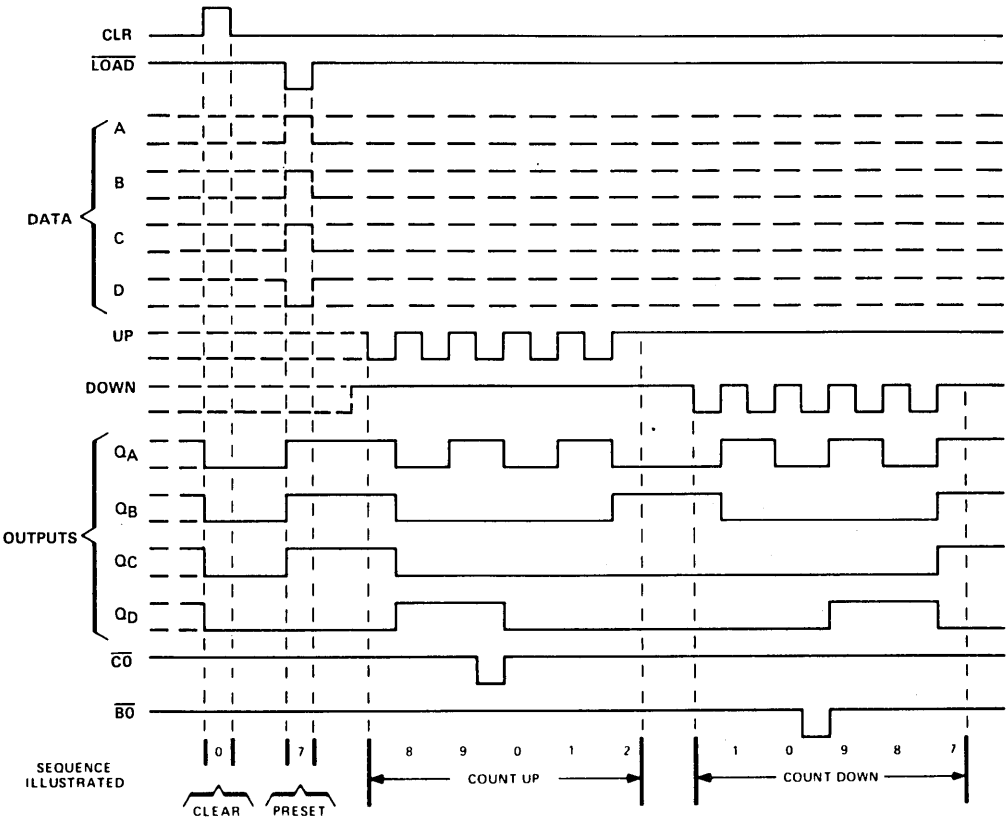


Pin numbers shown are for J and N packages.

typical clear, load, and count sequences

Illustrated below is the following:

1. Clear outputs to zero.
2. Load (preset) BCD seven.
3. Count up to eight, nine, carry, zero, one, and two.
4. Count down to one, zero, borrow, nine, eight, and seven.



NOTES: A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

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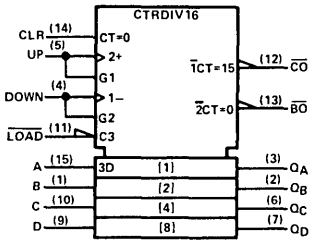
'HC193 logic symbol

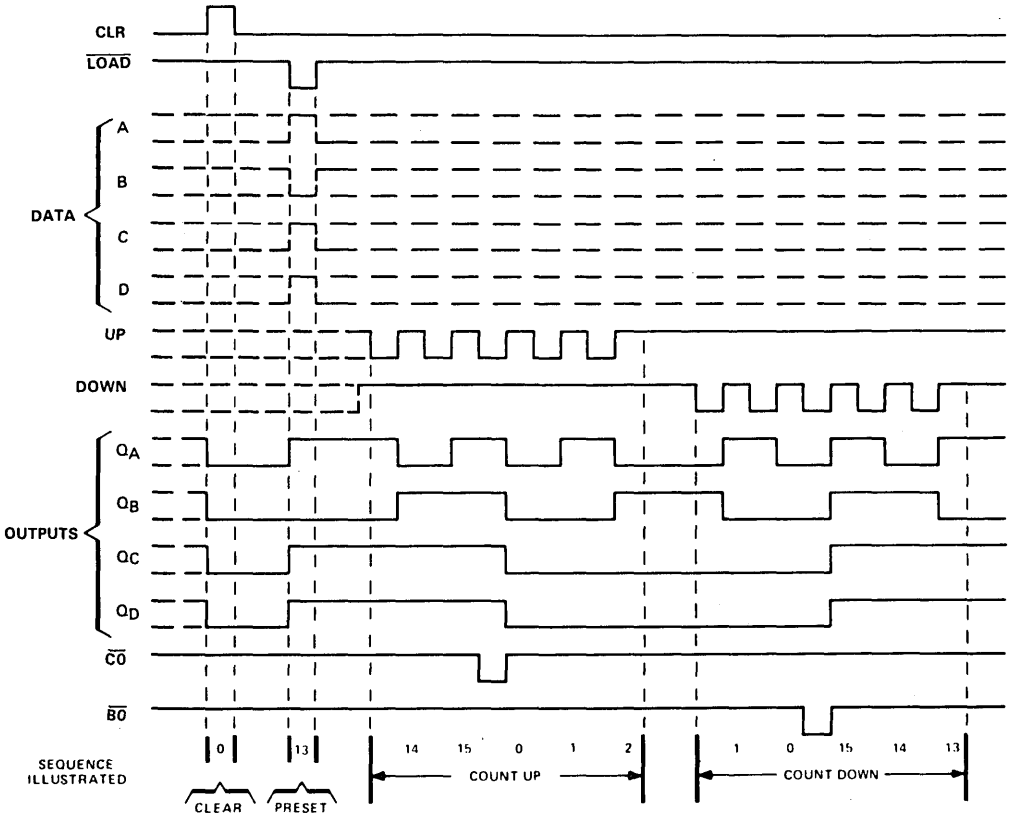


Pin numbers shown are for J and N packages.

typical clear, load, and count sequences

Illustrated below is the following:

1. Clear outputs to zero.
2. Load (preset) to binary thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.



NOTES: A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

timing requirements (supplement to recommended operating conditions)

			SN54HC192 SN54HC193			SN74HC192 SN74HC193			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}	Clock frequency	'HC 192							MHz
		'HC193							
t_w	Pulse duration	CLR high							ns
		$\overline{LOAD}$ low							
		UP or DOWN high							
		UP or DOWN low							
t_{su}	Setup time	Data before $\overline{LOAD}$↑							ns
		CLR inactive before UP↑ or DOWN↑							
		$\overline{LOAD}$ inactive before UP↑ or DOWN↑							
t_h	Hold time	Data after $\overline{LOAD}$↑							ns
		UP high after DOWN↑							
		DOWN high after UP↑							

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF				UNIT
						T_A = 25°C		SN54HC192 SN54HC193	SN74HC192 SN74HC193	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN MAX	
f_{max}	'HC192									MHz
	'HC193									
t_{PLH}	UP	$\overline{CO}$								ns
t_{PHL}										
t_{PLH}	DOWN	$\overline{BO}$								ns
t_{PHL}										
t_{PLH}	UP or DOWN	Any Q								ns
t_{PHL}										
t_{PLH}	$\overline{LOAD}$	Any Q								ns
t_{PHL}										
t_{PHL}	CLR	Any Q								ns

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

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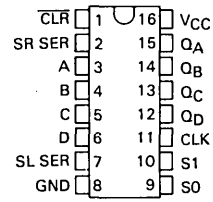
TYPES SN54HC194, SN74HC194
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

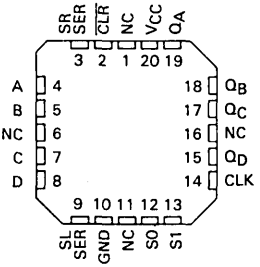
D2684, DECEMBER 1982

- Parallel Inputs and Outputs
- Four Operating Modes:
  - Synchronous Parallel Load
  - Right Shift
  - Left Shift
  - Do Nothing
- Positive Edge-Triggered Clocking
- Direct Overriding Clear
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54HC194 . . . J PACKAGE
SN74HC194 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC194 . . . FH OR FK PACKAGE
SN74HC194 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

These bidirectional shift registers are designed to incorporate virtually all of the features a system designer may want in a shift register. The circuit features parallel inputs, parallel outputs, right-shift and left-shift inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Parallel (broadside) load
Shift right (in the direction Q_A toward Q_D)
Shift left (in the direction Q_D toward Q_A)
Inhibit clocking (do nothing)

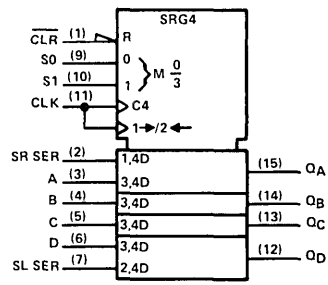
Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the shift register is inhibited when both mode control inputs are low.

The SN54HC194 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC194 is characterized for operation from −40°C to 85°C.

logic symbol

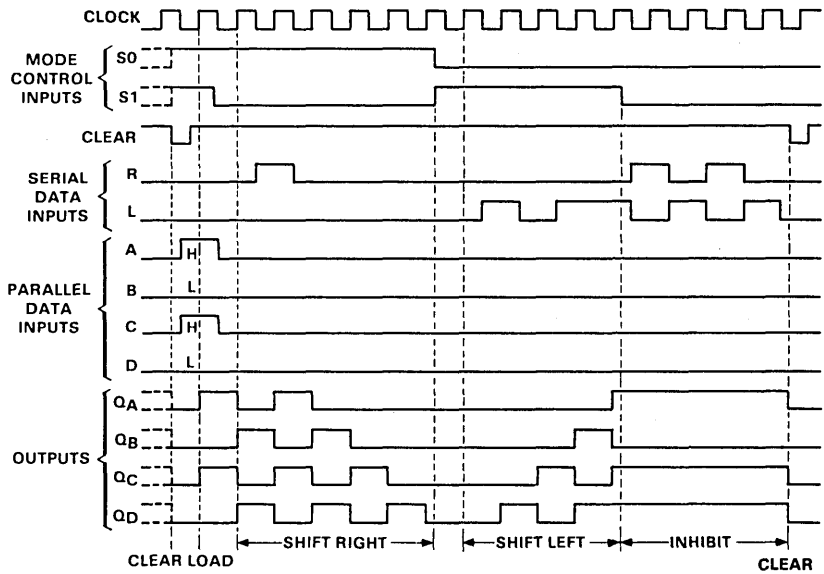


Pin numbers shown are for J and N packages.

FUNCTION TABLE

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{D0}

typical clear, load, right-shift, left-shift, inhibit, and clear sequences



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maximum ratings, recommended operating conditions, and electrical characteristics

See Table IV, page 2-6.

timing requirements (supplement to recommended operating conditions)

			SN54HC194			SN74HC194			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	CLK high or low							ns
		$\overline{CLR}$ low							
t_{su}	Setup time before CLK↑	Mode control							ns
		Serial and parallel data							
		$\overline{CLR}$ inactive							
t_h	Hold time at any input after CLK↑								ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF					UNIT
						T_A = 25°C			SN54HC194	SN74HC194	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN MAX	MIN MAX	
f_{max}											MHz
t_{PHL}	$\overline{CLR}$	Any Q									ns
t_{PLH}	CLK	Any Q									ns
t_{PHL}											

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	pF typ

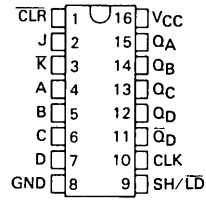
NOTE 1: For load circuit and voltage waveforms, see page 1-14.

TYPES SN54HC195, SN74HC195
4-BIT PARALLEL-ACCESS SHIFT REGISTERS

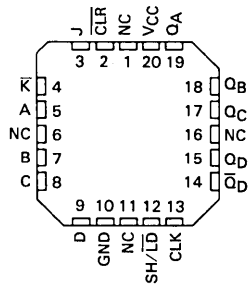
D2684, DECEMBER 1982

- **Synchronous Parallel Load**
- **Positive-Edge-Triggered Clocking**
- **J and $\overline{K}$ Inputs to First Stage**
- **Complementary Outputs from Last Stage**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC195 . . . J PACKAGE
SN74HC195 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC195 . . . FH OR FK PACKAGE
SN74HC195 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

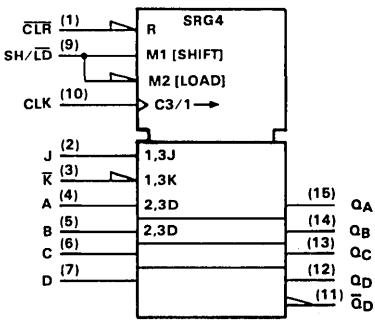
These 4-bit registers feature parallel inputs, parallel outputs, J-K serial inputs, shift/load control input, and a direct overriding clear. The registers have two modes of operation: parallel (broadside) load, and shift (in the direction Q_A toward Q_D).

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-K inputs. These inputs permit the first stage to perform as a J-K, D-, or T-type flip-flop as shown in the function table.

The SN54HC195 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC195 is characterized for operation from −40°C to 85°C.

logic symbol



Pin numbers shown are for J and N packages.

FUNCTION TABLE

INPUTS									OUTPUTS				
CLEAR	SHIFT/ LOAD	CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

3

PRODUCT PREVIEW

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TEXAS INSTRUMENTS
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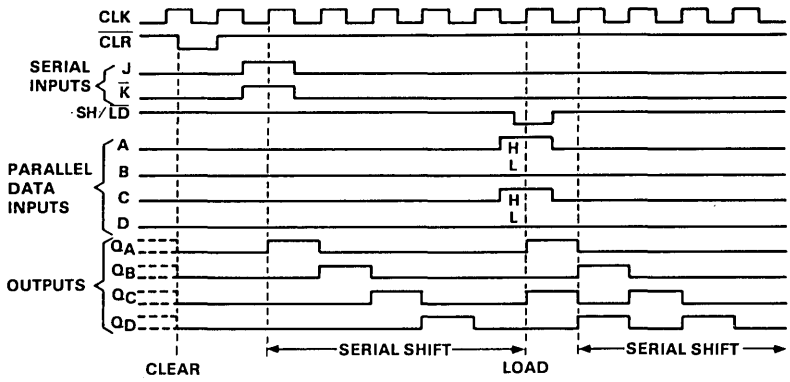
typical clear, shift, and load sequences



maximum ratings, recommended operating conditions, and electrical characteristics

See Table IV, page 2-6.

timing requirements (supplement to recommended operating conditions)

			SN54HC195			SN74HC195			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	CLK high or low							ns
		$\overline{CLR}$ low							
t_{su}	Setup time before CLK↑	SH/$\overline{LD}$							ns
		Serial and parallel data							
		$\overline{CLR}$ inactive (high)							
t_h	Hold time after CLK↑	SH/$\overline{LD}$							ns
		Serial and parallel data							

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF					UNIT
						T_A = 25°C			SN54HC195	SN74HC195	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN MAX	MIN MAX	
f_{max}											MHz
t_{PLH}	CLK	Q_A thru Q_D									ns
t_{PHL}											
t_{PLH}	CLK	$\overline{Q}_D$									ns
t_{PHL}											
t_{PLH}	$\overline{CLR}$	$\overline{Q}_D$									ns
t_{PHL}		Q_A thru Q_D									

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	pF typ

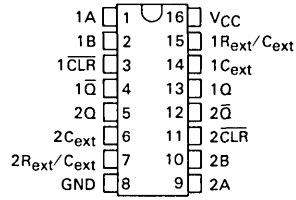
NOTE 1: For load circuit and voltage waveforms, see page 1-14.

TYPES SN54HC221, SN74HC221
DUAL MONOSTABLE MULTIVIBRATORS
WITH SCHMITT-TRIGGER INPUTS

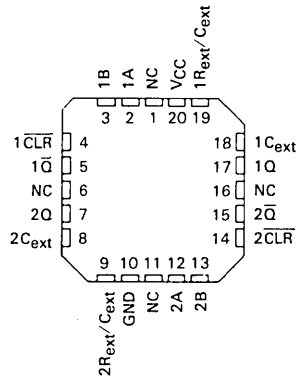
D2684, DECEMBER 1982

- **Overriding Clear Terminates Output Pulse**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC221 . . . J PACKAGE
SN74HC221 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC221 . . . FH OR FK PACKAGE
SN74HC221 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

These devices are monolithic dual multivibrators featuring a negative-transition-triggered input and a positive-transition-triggered input either of which can be used as an inhibit input.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry for the B input allows jitter-free triggering from inputs with slow transition rates.

Once fired, the outputs are independent of further transitions of the A and B inputs and are a function of the timing components, or the output pulses can be terminated by the overriding clear. Input pulses may be of any duration relative to the output pulse. Output rise and fall times are independent of pulse length.

Pulse duration stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will be limited only by the accuracy of external timing components.

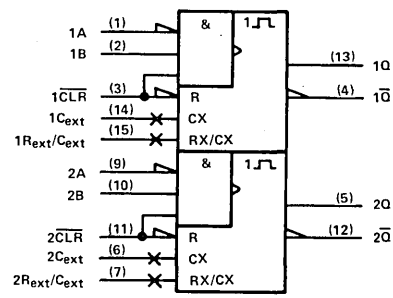
The SN54HC221 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC221 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(EACH MONOSTABLE)

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L†	H†
X	X	L	L†	H†
H	L	↑	⎍	⎍
H	↓	H	⎍	⎍
↑	L	H	⎍	⎍

†The second and third lines each indicate the logic levels the outputs will take on after the completion of any pulse already started.

logic symbol



PRODUCT PREVIEW

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TEXAS INSTRUMENTS
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maximum ratings, recommended operating conditions, and electrical characteristics

See Table IV, page 2-6.

Note: The minimum recommended supply voltage for this device is 3 V.

timing requirements (supplement to recommended operating conditions)

			SN54HC221			SN74HC221			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
dv/dt	Rate of rise or fall of input pulse	A inputs							V/μS
		B inputs							V/S
t_w	Input pulse duration	A or B							ns
		$\overline{CLR}$ low							
t_{su}	Setup time, $\overline{CLR}$ inactive								ns
R_{ext}	External timing resistance								kΩ
C_{ext}	External timing capacitance								μF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TIMING COMPONENTS		V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF					UNIT
								T_A = 25°C			SN54HC221	SN74HC221	
			C_{ext}	R_{ext}	MIN	TYP	MAX	MIN	TYP	MAX	MIN MAX	MIN MAX	
t_{PLH}	A	Q	80 pF	2 kΩ									ns
	B												
t_{PHL}	A	$\overline{Q}$	80 pF	2 kΩ									ns
	B												
t_{PHL}	$\overline{CLR}$	Q	80 pF	2 kΩ									ns
t_{PLH}		$\overline{Q}$											
$t_{w(out)}$	A or B	Q or $\overline{Q}$	80 pF	2 kΩ									ns
			0 pF	2 kΩ									
			100 pF	10 kΩ									
			1 μF	10 kΩ									ms

C_{pd}	Power dissipation capacitance per multivibrator	No load, T_A = 25°C	pF typ

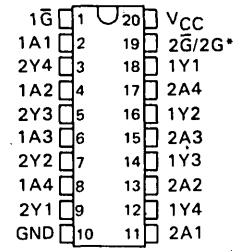
NOTE 1: For load circuit and voltage waveforms, see page 1-14.

TYPES SN54HC240, SN54HC241, SN74HC240, SN74HC241 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

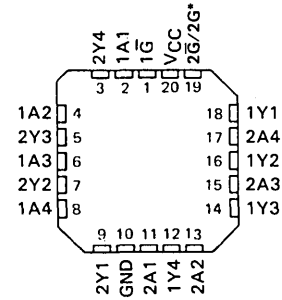
D2684, DECEMBER 1982

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **High-Current Outputs Drive up to 15 LSTTL Loads**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC' . . . J PACKAGE
SN74HC' . . . J OR N PACKAGE
(TOP VIEW)



SN54HC' . . . FH OR FK PACKAGE
SN74HC' . . . FH OR FN PACKAGE
(TOP VIEW)



*2G̅ for 'HC240, or 2G for 'HC241

description

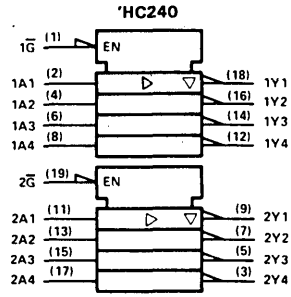
These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical G̅ (active-low output control) inputs, and complementary G and G̅ inputs. These devices feature high fan-out.

The SN54HC' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC' family is characterized for operation from −40°C to 85°C.

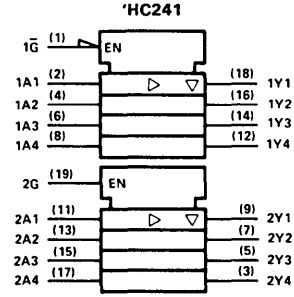
3

logic symbols

'HC240



'HC241



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table III, page 2-5.

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'HC240 switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 45 pF, R_L = 667Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, See Note 1			UNIT
				T_A = 25°C	SN54HC240	SN74HC240	
			MIN TYP MAX	MIN TYP MAX	MIN MAX	MIN MAX	
t_{PLH}	A	Y					ns
t_{PHL}							
t_{PZH}	$\overline{G}$	Y					ns
t_{PZL}							
t_{PLZ}	$\overline{G}$	Y					ns
t_{PLZ}							
C_{pd}	Power dissipation capacitance per buffer			No load, T_A = 25°C		pF typ	

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

'HC241 switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 45 pF, R_L = 667Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, See Note 1			UNIT
				T_A = 25°C	SN54HC241	SN74HC241	
			MIN TYP MAX	MIN TYP MAX	MIN MAX	MIN MAX	
t_{PLH}	A	Y					ns
t_{PHL}							
t_{PZH}	$1\overline{G}$	1Y					ns
t_{PZL}							
t_{PHZ}	$1\overline{G}$	1Y					ns
t_{PLZ}							
t_{PZH}	2G	2Y					ns
t_{PZL}							
t_{PHZ}	2G	2Y					ns
t_{PLZ}							
C_{pd}	Power dissipation capacitance per buffer			No load, T_A = 25°C		pF typ	

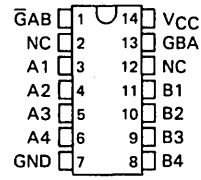
NOTE 1: For load circuit and voltage waveforms, see page 1-14.

TYPES SN54HC242, SN54HC243, SN74HC242, SN74HC243 QUADRUPLE BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

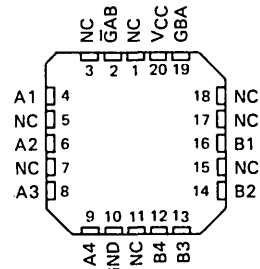
D2684, DECEMBER 1982

- 2-Way Asynchronous Communication Between Data Buses
- High-Current Outputs Can Drive up to 15 LSTTL Loads
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54HC242, SN54HC243 . . . J PACKAGE
SN74HC242, SN74HC243 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC242, SN54HC243 . . . FH OR FK PACKAGE
SN74HC242, SN74HC243 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

These four-data-line transceivers are designed for asynchronous two-way communications between data buses. The SN74HC' devices can be used to drive terminated lines down to 133 ohms.

The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from −40°C to 85°C.

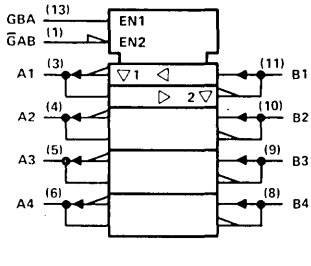
3

FUNCTION TABLE

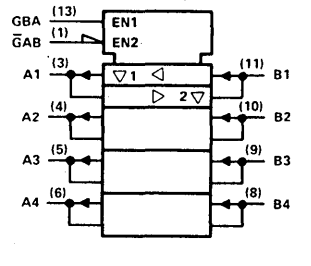
INPUTS		'HC242	'HC243
$\overline{G}AB$	GBA		
L	L	$\overline{A}$ to B	A to B
H	H	$\overline{B}$ to A	B to A
H	L	Isolation	Isolation
L	H	Latch A and B ($A = \overline{B}$)	Latch A and B ($A = B$)

logic symbol

'HC242



'HC243



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table III, page 2-5.

PRODUCT PREVIEW

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INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

'HC242 switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 45 pF, R_L = 667Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, See Note 1			UNIT
						T_A = 25°C		SN54HC242 SN74HC242	
			MIN	TYP	MAX	MIN	TYP MAX	MIN MAX	MIN MAX	
t_{PLH}	A or B	B or A								ns
t_{PHL}										
t_{PZH}	$\overline{G}$AB	B								ns
t_{PZL}										
t_{PHZ}	$\overline{G}$AB	B								ns
t_{PLZ}										
t_{PZH}	GBA	A								ns
t_{PZL}										
t_{PHZ}	GBA	A								ns
t_{PLZ}										

C_{pd}	Power dissipation capacitance per transceiver	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

3

'HC243 switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 45 pF, R_L = 667Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, See Note 1			UNIT
						T_A = 25°C		SN54HC243 SN74HC243	
			MIN	TYP	MAX	MIN	TYP MAX	MIN MAX	MIN MAX	
t_{PLH}	A or B	B or A								ns
t_{PHL}										
t_{PZH}	$\overline{G}$AB	B								ns
t_{PZL}										
t_{PHZ}	$\overline{G}$AB	B								ns
t_{PLZ}										
t_{PZH}	GBA	A								ns
t_{PZL}										
t_{PHZ}	GBA	A								ns
t_{PLZ}										

C_{pd}	Power dissipation capacitance per transceiver	No load, T_A = 25°C	pF typ

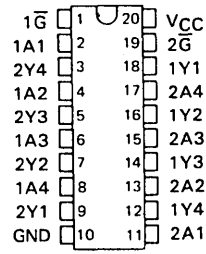
NOTE 1: For load circuit and voltage waveforms, see page 1-14.

TYPES SN54HC244, SN74HC244
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

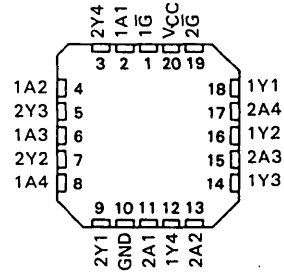
D2684, DECEMBER 1982

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **High-Current Outputs Can Drive up to 15 LSTTL Loads**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC244 . . . J PACKAGE
SN74HC244 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC244 . . . FH OR FK PACKAGE
SN74HC244 . . . FH OR FN PACKAGE
(TOP VIEW)



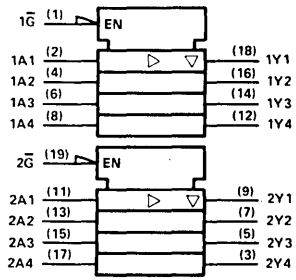
description

These octal buffers and line drivers are designed specifically to improve both the performance and density of the three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'HC240 and 'HC241, these devices provide the choice of selected combinations of inverting outputs, symmetrical $\overline{G}$ (active-low input control) inputs, and complementary G and $\overline{G}$ inputs.

The SN54HC244 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC244 is characterized for operation from −40°C to 85°C.

3

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table III, page 2-5.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 45 pF, R_L = 667Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, See Note 1				UNIT
						T_A = 25°C		SN54HC244	SN74HC244	
			MIN	TYP	MAX	MIN	TYP MAX	MIN MAX	MIN MAX	
t_{PLH}	A	Y								ns
t_{PHL}										
t_{PZH}	$\overline{G}$	Y								ns
t_{PZL}										
t_{PLZ}	$\overline{G}$	Y								ns
t_{PHZ}										

C_{pd}	Power dissipation capacitance per buffer	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

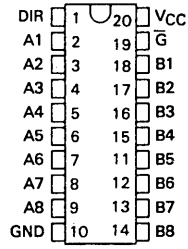
3

TYPES SN54HC245, SN74HC245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

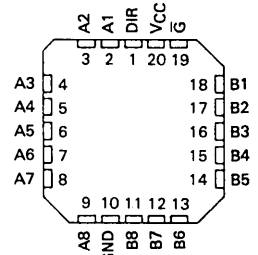
D2684, DECEMBER 1982

- **High-Current 3-State Outputs Drive Bus Lines Directly or Up to 15 LSTTL Loads**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC245 . . . J PACKAGE
SN74HC245 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC245 . . . FH OR FK PACKAGE
SN74HC245 . . . FH OR FN PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for synchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

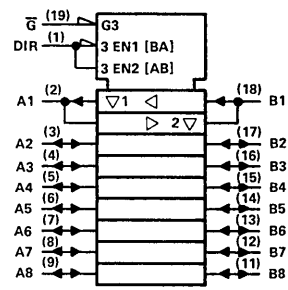
The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

The SN54HC245 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74HC245 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

CONTROL INPUTS		OPERATION
$\overline{G}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table III, page 2-5.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 45 pF, R_L = 667Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, See Note 1				UNIT
						T_A = 25°C		SN54HC245	SN74HC245	
			MIN	TYP	MAX	MIN	TYP MAX	MIN MAX	MIN MAX	
t_{PLH}	A or B	B or A								ns
t_{PHL}										
t_{PZH}	$\overline{G}$	A or B								ns
t_{PZL}										
t_{PHZ}	$\overline{G}$	A or B								ns
t_{PLZ}										

C_{pd}	Power dissipation capacitance per transceiver	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

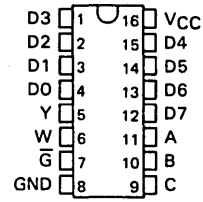
3

TYPES SN54HC251, SN74HC251 DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

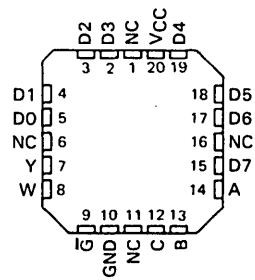
D2684, DECEMBER 1982

- **3-State Version of 'HC151**
- **High-Current 3-State Outputs Interface Directly with System Bus or Can Drive up to 15 LSTTL Loads**
- **Performs Parallel-to-Serial Conversion**
- **Complementary Outputs Provide True and Inverted Data**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC251 . . . J PACKAGE
SN74HC251 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC251 . . . FH OR FK PACKAGE
SN74HC251 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

These data selectors/multiplexers contain full binary decoding to select one-of-eight data sources and feature strobe-controlled complementary three-state outputs.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state), the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Both outputs are controlled by the strobe ($\overline{G}$). The outputs are disabled when $\overline{G}$ is high.

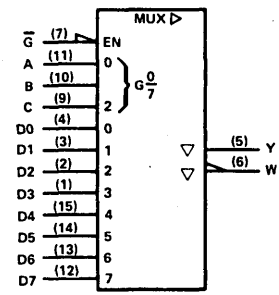
The SN54HC251 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC251 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE	Y	W
C	B	A	$\overline{G}$		
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

D0, D1 . . . D7 = the level of the respective D input

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table III, page 2-5.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 45 pF, R_L = 667Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, See Note 1				UNIT
						T_A = 25°C			SN54HC251	SN74HC251	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN MAX	MIN MAX	
t_{PLH}	A, B or C	Y									ns
t_{PHL}											
t_{PLH}	A, B or C	W									ns
t_{PHL}											
t_{PLH}	Any D	Y									ns
t_{PHL}											
t_{PLH}	Any D	W									ns
t_{PHL}											
t_{PZH}	$\overline{G}$	Y									ns
t_{PZL}											
t_{PZH}	$\overline{G}$	W									ns
t_{PZL}											
t_{PHZ}	$\overline{G}$	Y									ns
t_{PLZ}											
t_{PHZ}	$\overline{G}$	W									ns
t_{PLZ}											

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

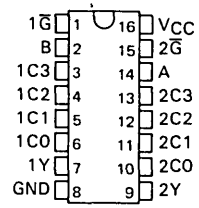
3

TYPES SN54HC253, SN74HC253
DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

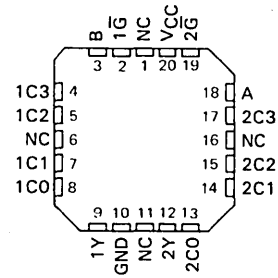
D2684, DECEMBER 1982

- **3-State Versions of 'HC153**
- **High-Current Outputs Drive up to 15 LSTTL Loads**
- **Permits Multiplexing from N Lines to 1 Line**
- **Performs Parallel-to-Serial Conversion**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC253 . . . J PACKAGE
SN74HC253 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC253 . . . FH OR FK PACKAGE
SN74HC253 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enabled output will drive the bus line to a high or low logic level. Each output has its own strobe ($\overline{G}$). The output is disabled when its strobe is high.

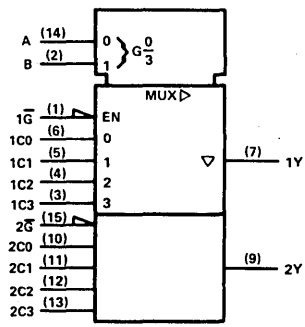
The SN54HC253 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC253 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections.

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table III, page 2-5.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 45 pF, R_L = 667Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, See Note 1				UNIT
						T_A = 25°C		SN54HC253	SN74HC253	
			MIN	TYP	MAX	MIN	TYP MAX	MIN MAX	MIN MAX	
t_{PLH}	A or B	Any Y								ns
t_{PHL}										
t_{PLH}	Data (Any C)	Y								ns
t_{PHL}										
t_{PZH}	$\overline{G}$	Y								ns
t_{PZL}										
t_{PHZ}	$\overline{G}$	Y								ns
t_{PLZ}										

C_{pd}	*Power dissipation capacitance per multiplexer*	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

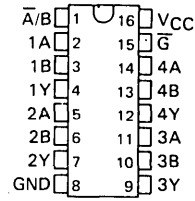
3

TYPES SN54HC257, SN54HC258, SN74HC257, SN74HC258 QUAD 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

D2684, DECEMBER 1982

- **High-Current 3-State Outputs Interface Directly with System Bus or Can Drive up to 15 LSTTL Loads**
- **Provides Bus Interface from Multiple Sources in High-Performance Systems**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC257, SN54HC258 . . . J PACKAGE
SN74HC257, SN74HC258 . . . J OR N PACKAGE
(TOP VIEW)

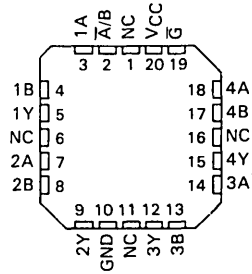


description

These devices are designed to multiplex signals from four-bit data sources to four-output data lines in bus-organized systems. The 3-state outputs will not load the data lines when the output control pin ($\overline{G}$) is at a high-logic level..

The SN54HC257 and SN54HC258 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC257 and SN74HC258 are characterized for operation from −40°C to 85°C.

SN54HC257, SN54HC258 . . . FH OR FK PACKAGE
SN74HC257, SN74HC258 . . . FH OR FN PACKAGE
(TOP VIEW)



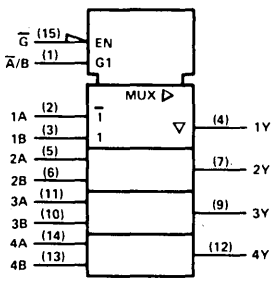
NC — No internal connection

FUNCTION TABLE

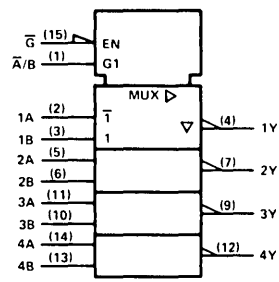
INPUTS				OUTPUT Y	
OUTPUT CONTROL $\overline{G}$	SELECT A/B	DATA A	DATA B	'HC257	'HC258
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

logic symbols

'HC257



'HC258



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table III, page 2-5.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

'HC257 switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 45 pF, R_L = 667Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, See Note 1				UNIT
				T_A = 25°C		SN54HC257	SN74HC257	
			MIN TYP MAX	MIN TYP MAX		MIN MAX	MIN MAX	
t_{PLH}	A or B	Any Y						ns
t_{PHL}								
t_{PLH}	$\overline{A}$/B	Any Y						ns
t_{PHL}								
t_{PZH}	$\overline{G}$	Any Y						ns
t_{PZL}								
t_{PHZ}	$\overline{G}$	Any Y						ns
t_{PLZ}								

C_{pd}	Power dissipation capacitance per multiplexer	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

3

'HC258 switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 45 pF, R_L = 667 Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, See Note 1				UNIT
				T_A = 25°C		SN54HC258	SN74HC258	
			MIN TYP MAX	MIN TYP MAX		MIN MAX	MIN MAX	
t_{PLH}	A or B	Any Y						ns
t_{PHL}								
t_{PLH}	$\overline{A}$/B	Any Y						ns
t_{PHL}								
t_{PZH}	$\overline{G}$	Any Y						ns
t_{PZL}								
t_{PHZ}	$\overline{G}$	Any Y						ns
t_{PLZ}								

C_{pd}	Power dissipation capacitance per multiplexer	No load, T_A = 25°C	pF typ

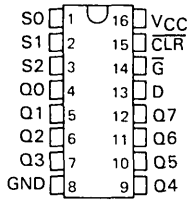
NOTE 1: For load circuit and voltage waveforms, see page 1-14.

TYPES SN54HC259, SN74HC259
8-BIT ADDRESSABLE LATCHES

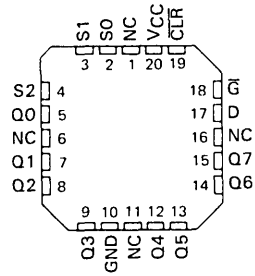
D2684, DECEMBER 1982

- 8-Bit Parallel-Out Storage Register Performs Serial-to-Parallel Conversion with Storage
- Asynchronous Parallel Clear
- Active-High Decoder
- Enable Input Simplifies Expansion
- Expandable for N-Bit Applications
- Four Distinct Functional Modes
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54HC259 . . . J PACKAGE
SN74HC259 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC259 . . . FH OR FK PACKAGE
SN74HC259 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

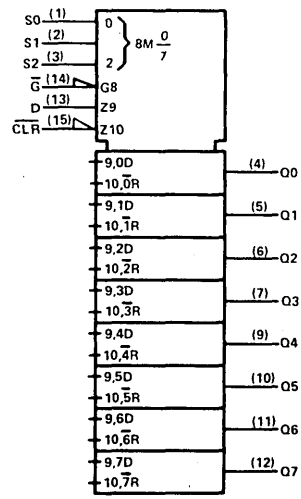
description

These 8-bit addressable latches are designed for general purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and active-high decoders or demultiplexers. They are multifunctional devices capable of storing single-line data in eight addressable latches, and being a 1-of-8 decoder or demultiplexer with active-high outputs.

Four distinct modes of operation are selectable by controlling the clear ($\overline{CLR}$) and enable ($\overline{G}$) inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in terminal is written into the addressed latch. The addressed latch will follow the data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latches, enable $\overline{G}$ should be held high (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode, the addressed output will follow the level of the D input with all other outputs low. In the clear mode, all outputs are low and unaffected by the address and data inputs.

The SN54HC259 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC259 is characterized for operation from −40°C to 85°C.

logic symbol



Pin numbers shown are for J and N packages.

FUNCTION TABLE

INPUTS CLR	INPUTS G	OUTPUT OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
H	L	D	Q_{i0}	Addressable Latch
H	H	Q_{i0}	Q_{i0}	Memory
L	L	D	L	8-Line Demultiplexer
L	H	L	L	Clear

LATCH SELECTION TABLE

SELECT INPUTS S2	S1	S0	LATCH ADDRESSED
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

maximum ratings, recommended operating conditions, and electrical characteristics

See Table IV, page 2-6.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
INCORPORATED
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timing requirements (supplement to recommended operating conditions)

			SN54HC259			SN74HC259			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
t_w	Pulse duration	$\overline{CLR}$ low							ns
		$\overline{G}$ low							
t_{su}	Setup time before $\overline{G}$↑								ns
t_h	Hold time after $\overline{G}$↑								ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF				UNIT
						T_A = 25°C		SN54HC259	SN74HC259	
			MIN	TYP	MAX	MIN	TYP MAX	MIN MAX	MIN MAX	
t_{PHL}	$\overline{CLR}$	Any Q								ns
t_{PLH}	Data	Any Q								ns
t_{PHL}										
t_{PLH}	Address	Any Q								ns
t_{PHL}										
t_{PLH}	$\overline{G}$	Any Q								ns
t_{PHL}										

C_{pd}	Power dissipation capacitance per latch	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

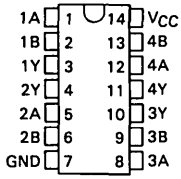
3

TYPES SN54HC266, SN74HC266
QUADRUPLE 2-INPUT EXCLUSIVE-NOR GATES

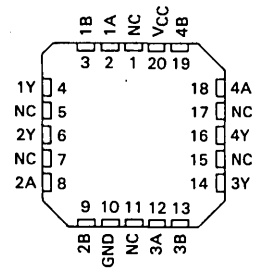
D2684, DECEMBER 1982

- **Can Be Used as a 4-Bit Digital Comparator**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC266 . . . J PACKAGE
SN74HC266 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC266 . . . FH OR FK PACKAGE
SN74HC266 . . . FH OR FN PACKAGE
(TOP VIEW)



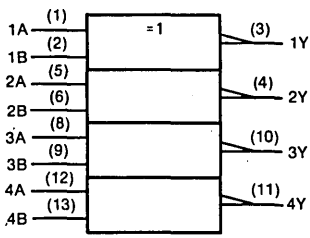
NC — No internal connection

description

The 'HC266 is composed of four independent 2-input exclusive-NOR gates. While pin-compatible with the 'LS266, the 'HC266 has totem-pole outputs rather than open-collector.

The SN54HC266 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC266 is characterized for operation from −40°C to 85°C.

logic symbol



Pin numbers shown are for J and N packages.

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

maximum ratings, recommended operating conditions, and electrical characteristics

See Table I, page 2-3.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF				UNIT
						T_A = 25°C			SN54HC266	SN74HC266	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN MAX	MIN MAX	
t_{PLH}	A or B	Y									ns
t_{PHL}											

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

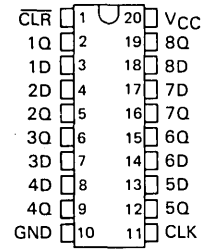
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TYPES SN54HC273, SN74HC273
OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

D2684, DECEMBER 1982

- Contains Eight Flip-Flops with Single-Rail Outputs
- Direct Clear Input
- Individual Data Input to Each Flip-Flop
- Applications Include:
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54HC273 . . . J PACKAGE
SN74HC273 . . . J OR N PACKAGE
(TOP VIEW)



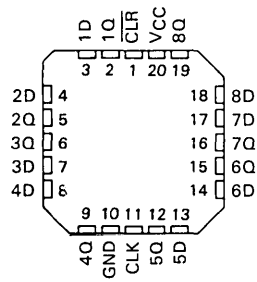
description

These circuits are positive-edge-triggered D-type flip-flops with a direct clear input.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering *occurs at a particular voltage level and is not* directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

The SN54HC273 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC273 is characterized for operation from −40°C to 85°C.

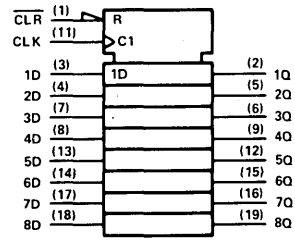
SN54HC273 . . . FH OR FK PACKAGE
SN74HC273 . . . FH OR FN PACKAGE
(TOP VIEW)



FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

logic symbol



Pin numbers shown are for all packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table IV, page 2-6.

timing requirements (supplement to recommended operating conditions)

			SN54HC273			SN74HC273			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	$\overline{CLR}$ low							ns
		CLK high							
		CLK low							
t_{su}	Setup time before CLK↑	Data							ns
		$\overline{CLR}$ inactive state							
t_h	Hold time, data after CLK↑								ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF					UNIT
						T_A = 25°C			SN54HC273	SN74HC273	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN MAX	MIN MAX	
f_{max}											MHz
t_{PHL}	$\overline{CLR}$	Any Q									ns
t_{PLH}	CLK	Any Q									ns
t_{PHL}											

C_{pd}	Power dissipation capacitance per flip-flop	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

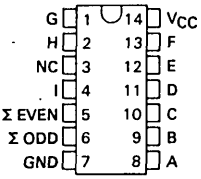
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TYPES SN54HC280, SN74HC280
9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

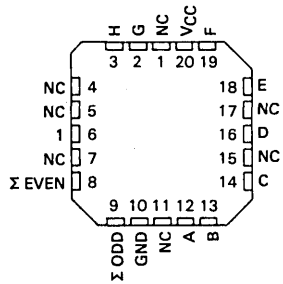
D2684, DECEMBER 1982

- Generates Either Odd or Even Parity for Nine Data Lines
- Cascadable for n-Bits
- Can Be Used to Upgrade Existing Systems Using MSI Parity Circuits
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54HC280 . . . J PACKAGE
SN74HC280 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC280 . . . FH OR FK PACKAGE
SN74HC280 . . . FH OR FN PACKAGE
(TOP VIEW)



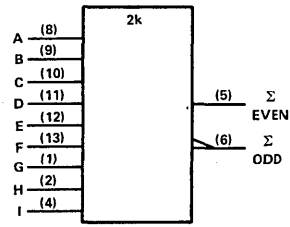
NC — No internal connection

description

These universal, monolithic, nine-bit parity generators/checkers feature odd and even outputs to facilitate operation of either odd or even parity application. The word-length capability is easily expanded by cascading.

The SN54HC280 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC280 is characterized for operation from −40°C to 85°C.

logic symbol



Pin numbers shown are for J and N packages.

FUNCTION TABLE

NUMBER OF INPUTS A THRU I THAT ARE HIGH	OUTPUTS	
	Σ EVEN	Σ ODD
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

maximum ratings, recommended operating conditions, and electrical characteristics

See Table IV, page 2-6.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF				UNIT
						T_A = 25°C			SN54HC280	SN74HC280	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN MAX	MIN MAX	
t_{PLH}	Data	Σ Even									ns
t_{PHL}											
t_{PLH}	Data	Σ Odd									ns
t_{PHL}											

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

3

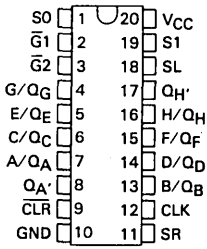
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TYPES SN54HC299, SN74HC299
8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS

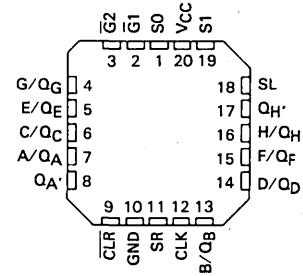
D2684, DECEMBER 1982

- **Multiplexed I/O Ports Provide Improved Bit Density**
- **Four Modes of Operation: Hold (Store), Shift Right, Shift Left, and Load Data**
- **High-Current 3-State Outputs Drive Bus Lines Directly or up to 15 LSTTL Loads**
- **Can Be Cascaded for N-Bit Word Lengths**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC299 . . . J PACKAGE
SN74HC299 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC299 . . . FH OR FK PACKAGE
SN74HC299 . . . FH OR FN PACKAGE
(TOP VIEW)



description

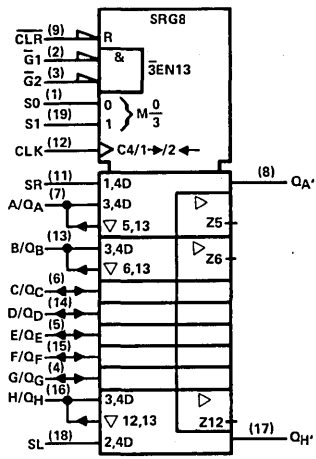
These eight-bit universal registers feature multiplexed I/O ports to achieve full eight-bit data handling in a single 20-pin package. 'HC299 applications are as stacked or push-down registers, buffer storage, and accumulator registers.

Two function-select inputs and two output control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines, S0 and S1, high. This places the three-state outputs in a high-impedance state, which permits data that is applied on the I/O ports to be clocked into the register. Reading out of this register can be accomplished while the outputs are enabled in any mode. A direct overriding input is provided to clear the register whether the outputs are enabled or off. Taking either of the output controls, $\overline{G}1$ or $\overline{G}2$, high disables the outputs but this has no effect on shifting or storage of data.

The SN54HC299 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74HC299 is characterized for operation from -40°C to 85°C.

logic symbol



Pin numbers shown are for J and N packages.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

FUNCTION TABLE

MODE	INPUTS								INPUTS/OUTPUTS								OUTPUTS	
	CLEAR	FUNCTION SELECT		OUTPUT CONTROL		CLOCK	SERIAL		A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	$Q_{A'}$	$Q_{H'}$
		S1	S0	$\overline{G1}$↑	$\overline{G2}$↑		SL	SR										
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L*	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
	H	L	H	L	L	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

†When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

a . . . h = the level of the steady-state input at inputs A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.

3

maximum ratings, recommended operating conditions, and electrical characteristics

See Table III, page 2-5.

timing requirements (supplement to recommended operating conditions)

			SN54HC299			SN74HC299			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	CLK high							ns
		CLK low							
		$\overline{CLR}$ low							
t_{su}	Setup time before CLK↑	Select							ns
		High-level data							
		Low-level data							
		$\overline{CLR}$ inactive-state							
t_h	Hold time after CLK↑	Select							ns
		Data							

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = Note 2, R_L = Note 2, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, See Note 1						UNIT
						T_A = 25°C			SN54HC299		SN74HC299	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}													MHz
t_{PLH}	CLK	Q_A' or Q_H'											ns
t_{PHL}													
t_{PHL}	$\overline{CLR}$	Q_A' or Q_H'											ns
t_{PLH}	CLK	Q_A thru Q_H											ns
t_{PHL}													
t_{PHL}	$\overline{CLR}$	Q_A thru Q_H											ns
t_{PZH}	$\overline{G1}$, $\overline{G2}$	Q_A thru Q_H											ns
t_{PZL}													
t_{PHZ}	$\overline{G1}$, $\overline{G2}$	Q_A thru Q_H											ns
t_{PLZ}													
t_{PZH}	S0, S1	Q_A thru Q_H											ns
t_{PZL}													
t_{PHZ}	S0, S1	Q_A thru Q_H											ns
t_{PLZ}													

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	pF typ

NOTES: 1. For load circuit and voltage waveforms, see page 1-14.
2. C_L = 15 pF, R_L = 2 kΩ for outputs Q_A' or Q_H';
C_L = 45 pF, R_L = 667 Ω for outputs Q_A thru Q_H.

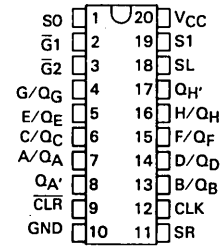
3

TYPES SN54HC323, SN74HC323 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS

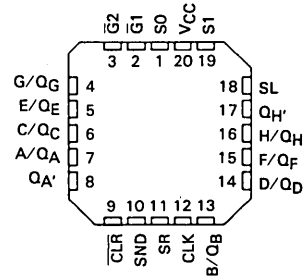
D2684, DECEMBER 1982

- Multiplexed I/O Ports Provide Improved Bit Density
- Four Modes of Operation: Hold (Store), Shift Right, Shift Left, and Load Data
- High-Current 3-State Outputs Drive Bus Lines Directly or up to 15 LSTTL Loads
- Can Be Cascaded for N-Bit Word Lengths
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54HC323 . . . J PACKAGE
SN74HC323 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC323 . . . FH OR FK PACKAGE
SN74HC323 . . . FH OR FN PACKAGE
(TOP VIEW)



description

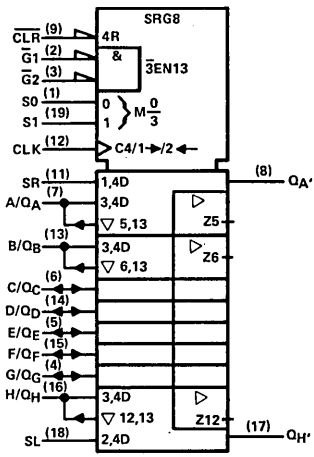
These eight-bit universal registers feature multiplexed I/O ports to achieve full eight bit data handling in a single 20-pin package. 'HC323 applications are as stacked or push-down registers, buffer storage, and accumulator registers.

Two function-select inputs and two output control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines S0 and S1, high. This places the three-state outputs in a high-impedance state, which permits data that is applied on the I/O ports to be clocked into the register. Reading out of this register can be accomplished while the outputs are enabled in any mode. The clear function is synchronous, and a low level at the clear input clears the register on the next low-to-high transition of the clock.

The SN54HC323 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74HC323 is characterized for operation from -40°C to 85°C.

logic symbol



Pin numbers shown are for J and N packages.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

FUNCTION TABLE

MODE	INPUTS								INPUTS/OUTPUTS								OUTPUTS	
	CLEAR	FUNCTION SELECT		OUTPUT CONTROL		CLOCK	SERIAL		A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	Q_A'	Q_H'
		S1	S0	$\overline{G1}$†	$\overline{G2}$†		SL	SR										
Clear	L	X	L	L	L	↑	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	↑	X	X	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	↑	X	X	X	X	X	X	X	X	X	X	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
	H	L	H	L	L	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

†When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

a . . . h = the level of the steady-state input at inputs A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table III, page 2-5.

3

timing requirements (supplement to recommended operating conditions)

			SN54HC323			SN74HC323			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	CLK high							ns
		CLK low							
t_{su}	Setup time before CLK↑	S0 or S1							ns
		Data							
		$\overline{CLR}$							
t_h	Hold time after CLK↑	S0 or S1							ns
		Data							
		$\overline{CLR}$							

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = Note 2, R_L = Note 2, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, See Note 1				UNIT
						T_A = 25°C			SN54HC323	SN74HC323	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN MAX	MIN MAX	
f_{max}											MHz
t_{PLH}	CLK	Q_A' or Q_H'									ns
t_{PHL}											
t_{PLH}	CLK	Q_A thru Q_H									ns
t_{PHL}											
t_{PZH}	$\overline{G1}$, $\overline{G2}$	Q_A thru Q_H									ns
t_{PZL}											
t_{PHZ}	$\overline{G1}$, $\overline{G2}$	Q_A thru Q_H									ns
t_{PLZ}											
t_{PZH}	S0 or S1	Q_A thru Q_H									ns
t_{PZL}											
t_{PHZ}	S0 or S1	Q_A thru Q_H									ns
t_{PLZ}											

C_{pd}	Power dissipation capacitance per register	No load, T_A = 25°C	pF typ

NOTES: 1. For load circuit and voltage waveforms, see page 1-14.
2. C_L = 45 pF and R_L = 667Ω for outputs Q_A thru Q_H;
C_L = 15 pF and R_L = 2kΩ for outputs Q_A' and Q_H'.

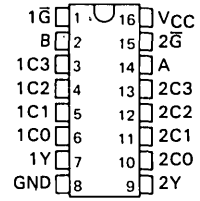
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TYPES SN54HC352, SN74HC352 DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

D2684, DECEMBER 1982

- Inverting Versions of 'HC153
- Permits Multiplexing from N Lines to 1 Line
- Performs Parallel-to-Serial Conversion
- Strobe (Enable) Line Provided for Cascading (N Lines to n Lines)
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54HC352 . . . J PACKAGE
SN74HC352 . . . J OR N PACKAGE
(TOP VIEW)

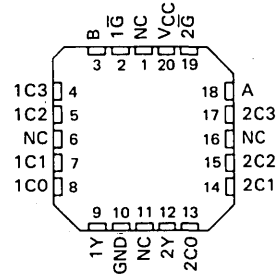


description

Each of these data selectors/multiplexers contains inverters and drivers to supply fully complementary binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs ($\overline{G}$) are provided for each of the two four-line sections.

The SN54HC352 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC352 is characterized for operation from −40°C to 85°C.

SN54HC352 . . . FH OR FK PACKAGE
SN74HC352 . . . FH OR FN PACKAGE
(TOP VIEW)



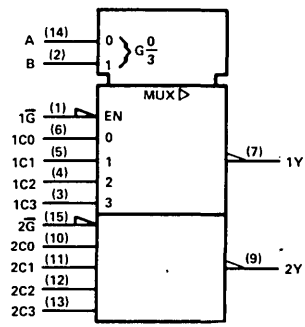
NC — No internal connection

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	H
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Select inputs A and B are common to both sections.

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table III, page 2-5.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, See Note 1			UNIT
				T_A = 25°C	SN54HC352	SN74HC352	
			MIN TYP MAX	MIN TYP MAX	MIN MAX	MIN MAX	
t_{PLH}	A or B	Y					ns
t_{PHL}							
t_{PLH}	Data (Any C)	Y					ns
t_{PHL}							
t_{PLH}	$\overline{G}$	Y					ns
t_{PHL}							

C_{pd}	Power dissipation capacitance per data selector	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

3

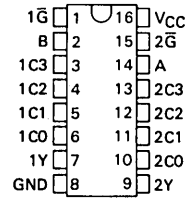
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TYPES SN54HC353, SN74HC353
DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

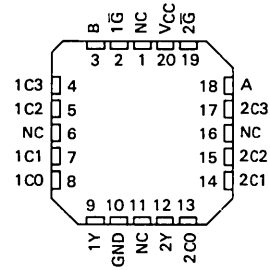
D2684, DECEMBER 1982

- Inverting Versions of 'HC253
- Permits Multiplexing from N Lines to 1 Line
- Performs Parallel-to-Serial Conversion
- High-Current Outputs Can Drive up to 15 LSTTL Loads
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54HC353 . . . J PACKAGE
SN74HC353 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC353 . . . FH OR FK PACKAGE
SN74HC353 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs ($\overline{G}$) are provided for each of the two four-line sections.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enable output will drive the bus line to a high or low logic level. Each output has its own strobe ($\overline{G}$). The output is disabled when its strobe is high.

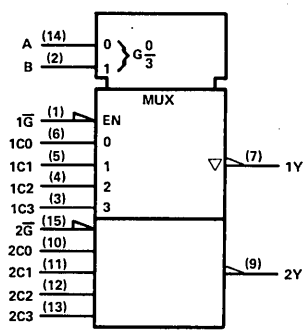
The SN54HC353 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC353 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Select inputs A and B are common to both sections.

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table III, page 2-5.

PRODUCT PREVIEW

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 45 pF, R_L = 667Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, See Note 1				UNIT
						T_A = 25°C		SN54HC353	SN74HC353	
			MIN	TYP	MAX	MIN	TYP MAX	MIN MAX	MIN MAX	
t_{PLH}	A or B	Y								ns
t_{PHL}										
t_{PLH}	Data (Any C)	Y								ns
t_{PHL}										
t_{PZH}	$\overline{G}$	Y								ns
t_{PZL}										
t_{PHZ}	$\overline{G}$	Y								ns
t_{PHL}										

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

3

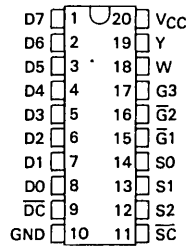
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TYPES SN54HC354, SN74HC354
8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS/ TRANSPARENT REGISTERS WITH 3-STATE OUTPUTS

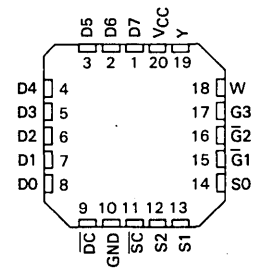
D2684, DECEMBER 1982

- Transparent Latches on Data Select Inputs
- Transparent Data Registers
- High-Current 3-State Outputs Can Drive up to 15 LSTTL Loads
- Complementary Outputs
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54HC354 . . . J PACKAGE
SN74HC354 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC354 . . . FH OR FK PACKAGE
SN74HC354 . . . FH OR FN PACKAGE
(TOP VIEW)

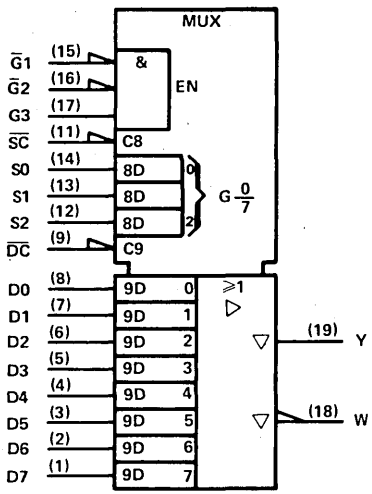


description

These monolithic data selectors/multiplexers contain full on-chip binary decoding to select one of eight data sources. The data-select is stored in transparent latches that are enabled by a low level on pin 11, $\overline{SC}$. A similar enable for data is obtained by a low level on pin 9, $\overline{DC}$.

The SN54HC354 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC354 is characterized for operation from −40°C to 85°C.

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table III, page 2-5.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

FUNCTION TABLE

INPUTS							OUTPUTS	
SELECT†			DATA CONTROL	OUTPUT ENABLES				
S2	S1	S0	$\overline{DC}$	$\overline{G1}$	$\overline{G2}$	G3	W	Y
X	X	X	X	H	X	X	Z	Z
X	X	X	X	X	H	X	Z	Z
X	X	X	X	X	X	L	Z	Z
L	L	L	L	L	L	H	$\overline{D0}$	D0
L	L	L	H	L	L	H	$\overline{D0}_n$	$D0_n$
L	L	H	L	L	L	H	$\overline{D1}$	D1
L	L	H	H	L	L	H	$\overline{D1}_n$	$D1_n$
L	H	L	L	L	L	H	$\overline{D2}$	D2
L	H	L	H	L	L	H	$\overline{D2}_n$	$D2_n$
L	H	H	L	L	L	H	$\overline{D3}$	D3
L	H	H	H	L	L	H	$\overline{D3}_n$	$D3_n$
H	L	L	L	L	L	H	$\overline{D4}$	D4
H	L	L	H	L	L	H	$\overline{D4}_n$	$D4_n$
H	L	H	L	L	L	H	$\overline{D5}$	D5
H	L	H	H	L	L	H	$\overline{D5}_n$	$D5_n$
H	H	L	L	L	L	H	$\overline{D6}$	D6
H	H	L	H	L	L	H	$\overline{D6}_n$	$D6_n$
H	H	H	L	L	L	H	$\overline{D7}$	D7
H	H	H	H	L	L	H	$\overline{D7}_n$	$D7_n$

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
Z = high-impedance state (off state)
↑ = transition from low to high level
D0 . . . D7 = the level of stead-state inputs at inputs D0 through D7, respectively
$D0_n$ . . . $D7_n$ = the level of steady state inputs at inputs D0 through D7, respectively, before the most recent low-to-high transition of data control
†This column shows the input address setup with $\overline{SC}$ low.

3

timing requirements (supplement to recommended operating conditions)

			SN54HC354			SN74HC354			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
t_{su}	Setup time (with respect to ↑ at pin 9)	High-level or low-level data							ns
t_h	Hold time (with respect to ↑ at pin 9)	High-level or low-level data							ns

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 45 pF, R_L = 667Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, See Note 1						UNIT
						T_A = 25°C			SN54HC354		SN74HC354	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D0-D7	Y											ns
t_{PHL}													
t_{PLH}		W											
t_{PHL}													
t_{PLH}	$\overline{DC}$	Y											ns
t_{PHL}													
t_{PLH}		W											
t_{PHL}													
t_{PLH}	S0, S1, S2	Y											ns
t_{PHL}													
t_{PLH}		W											
t_{PHL}													
t_{PLH}	$\overline{SC}$	Y											ns
t_{PHL}													
t_{PLH}		W											
t_{PHL}													
t_{PZH}	$\overline{G1}$, $\overline{G2}$	Y											ns
t_{PZL}													
t_{PHZ}													
t_{PLZ}													
t_{PZH}		W											
t_{PZL}													
t_{PHZ}													
t_{PLZ}													
t_{PZH}	G3	Y											ns
t_{PZL}													
t_{PHZ}													
t_{PLZ}													
t_{PZH}		W											
t_{PZL}													
t_{PHZ}													
t_{PLZ}													

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

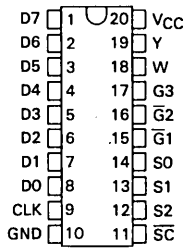
3

TYPES SN54HC356, SN74HC356
8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS/ EDGE-TRIGGERED REGISTERS WITH 3-STATE OUTPUTS

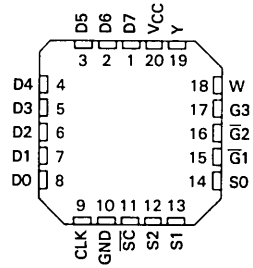
D2684, DECEMBER 1982

- **Transparent Latches on Data Select Inputs**
- **Edge-Triggered Data Registers**
- **High-Current 3-State Outputs Can Drive up to 15 LSTTL Loads**
- **Complementary Outputs**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC356 . . . J PACKAGE
SN74HC356 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC356 . . . FH OR FK PACKAGE
SN74HC356 . . . FH OR FN PACKAGE
(TOP VIEW)

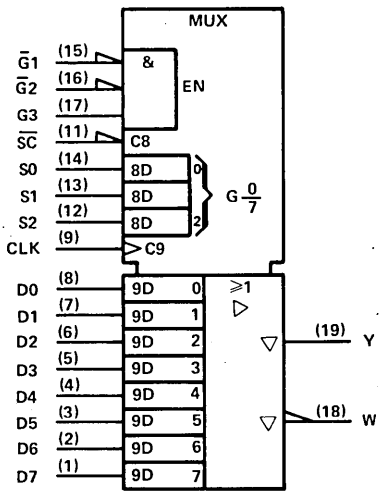


description

These monolithic data selectors/multiplexers contain full on-chip binary decoding to select one of eight data sources. The data-select address is stored in transparent latches that are enabled by a low level on pin 11, $\overline{SC}$. The edge-triggered data registers are clocked by a low-to-high transition on pin 9, CLK. Both true and complementary outputs are available.

The SN54HC356 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC356 is characterized for operation from −40°C to 85°C.

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table III, page 2-5.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

FUNCTION TABLE

INPUTS							OUTPUTS	
SELECT†			CLOCK	OUTPUT ENABLES				
S2	S1	S0		$\overline{G1}$	$\overline{G2}$	G3	W	Y
X	X	X	X	H	X	X	Z	Z
X	X	X	X	X	H	X	Z	Z
X	X	X	X	X	X	L	Z	Z
L	L	L	↑	L	L	H	$\overline{D0}$	D0
L	L	L	H or L	L	L	H	$\overline{D0}_n$	$D0_n$
L	L	H	↑	L	L	H	$\overline{D1}$	D1
L	L	H	H or L	L	L	H	$\overline{D1}_n$	$D1_n$
L	H	L	↑	L	L	H	$\overline{D2}$	D2
L	H	L	H or L	L	L	H	$\overline{D2}_n$	$D2_n$
L	H	H	↑	L	L	H	$\overline{D3}$	D3
L	H	H	H or L	L	L	H	$\overline{D3}_n$	$D3_n$
H	L	L	↑	L	L	H	$\overline{D4}$	D4
H	L	L	H or L	L	L	H	$\overline{D4}_n$	$D4_n$
H	L	H	↑	L	L	H	$\overline{D5}$	D5
H	L	H	H or L	L	L	H	$\overline{D5}_n$	$D5_n$
H	H	L	↑	L	L	H	$\overline{D6}$	D6
H	H	L	H or L	L	L	H	$\overline{D6}_n$	$D6_n$
H	H	H	↑	L	L	H	$\overline{D7}$	D7
H	H	H	H or L	L	L	H	$\overline{D7}_n$	$D7_n$

†This column shows the input address setup with $\overline{SC}$ low.

3

timing requirements (supplement to recommended operating conditions)

			SN54HC356			SN74HC356			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}	Clock frequency								MHz
t_{su}	Setup time before CLK↑	High-level or low-level data							ns
t_h	Hold time after CLK↑	High-level or low-level data							ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 45 pF, R_L = 667Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, See Note 1				UNIT
						T_A = 25°C		SN54HC356	SN74HC356	
			MIN	TYP	MAX	MIN	TYP MAX	MIN MAX	MIN MAX	
f_{max}										MHz
t_{PLH}	D0-D7	Y								ns
t_{PHL}										
t_{PLH}		W								
t_{PHL}										
t_{PLH}	CLK	Y								ns
t_{PHL}										
t_{PLH}		W								
t_{PHL}										
t_{PLH}	S0, S1, S2	Y								ns
t_{PHL}										
t_{PLH}		W								
t_{PHL}										
t_{PLH}	$\overline{SC}$	Y								ns
t_{PHL}										
t_{PLH}		W								
t_{PHL}										
t_{PZH}	$\overline{G1}$, $\overline{G2}$	Y								ns
t_{PZL}										
t_{PHZ}										
t_{PLZ}										
t_{PZH}		W								
t_{PZL}										
t_{PHZ}										
t_{PLZ}										
t_{PZH}	G3	Y								ns
t_{PZL}										
t_{PHZ}										
t_{PLZ}										
t_{PZH}		W								
t_{PZL}										
t_{PHZ}										
t_{PLZ}										

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

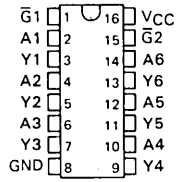
TYPES SN54HC365 THRU SN54HC368, SN74HC365 THRU SN54HC368 HEX BUS DRIVERS WITH 3-STATE OUTPUTS

D2684, DECEMBER 1982

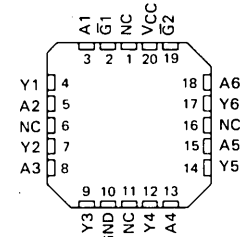
- **High-Current 3-State Outputs Drive Bus Lines, Buffer Memory Address Registers, or up to 15 LSTTL Loads**
- **Choice of True or Inverting Outputs**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

'HC365, 'HC367	True Outputs
'HC366, 'HC368	Inverting Outputs

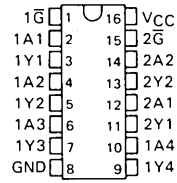
SN54HC365, SN54HC366 . . . J PACKAGE
SN74HC365, SN74HC366 . . . J OR N PACKAGE
(TOP VIEW)



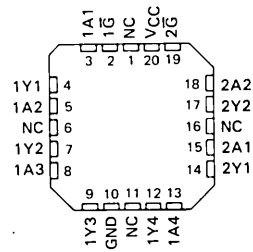
SN54HC367, SN54HC368 . . . FH OR FK PACKAGE
SN74HC367, SN74HC368 . . . FH OR FN PACKAGE
(TOP VIEW)



SN54HC367, SN54HC368 . . . J PACKAGE
SN74HC367, SN74HC368 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC365, SN54HC366 . . . FH OR FK PACKAGE
SN74HC368, SN74HC366 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

These Hex buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical G (active-low control) inputs.

The SN54' family is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74' family is characterized for operation from -40°C to 85°C.

maximum ratings, recommended operating conditions, and electrical characteristics

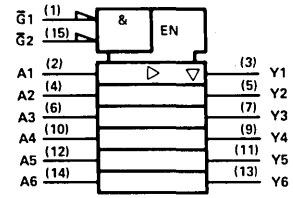
See Table III, page 2-5.

PRODUCT PREVIEW

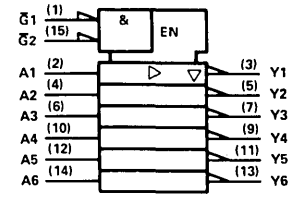
This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

logic symbols

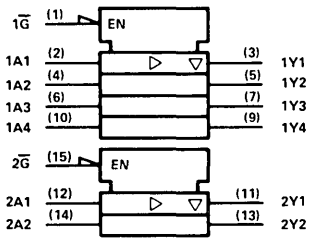
'HC365



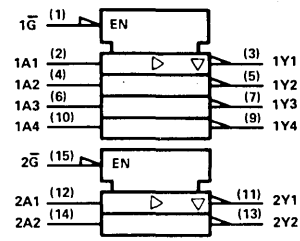
'HC366



'HC367



'HC368



Pin numbers shown are for J and N packages.

3

'HC365, 'HC367 switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 45 pF, R_L = 667Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, See Note 1			UNIT
				T_A = 25°C	SN54HC365 SN54HC367	SN74HC365 SN74HC367	
			MIN TYP MAX	MIN TYP MAX	MIN MAX	MIN MAX	
t_{PLH}	A	Y					ns
t_{PHL}							
t_{PZH}	$\overline{G}$	Y					ns
t_{PZL}							
t_{PHZ}	$\overline{G}$	Y					ns
t_{PLZ}							

C_{pd}	Power dissipation capacitance per driver	No load, T_A = 25°C	pF typ

'HC366, 'HC368 switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 45 pF, R_L = 667Ω, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, See Note 1			UNIT
				T_A = 25°C	SN54HC366 SN54HC368	SN74HC366 SN74HC368	
			MIN TYP MAX	MIN TYP MAX	MIN MAX	MIN MAX	
t_{PLH}	A	Y					ns
t_{PHL}							
t_{PZH}	$\overline{G}$	Y					ns
t_{PZL}							
t_{PHZ}	$\overline{G}$	Y					ns
t_{PLZ}							

C_{pd}	Power dissipation capacitance per driver	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

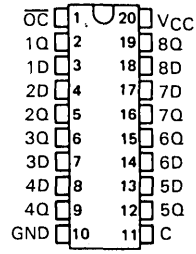
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TYPES SN54HC373, SN74HC373
OCTAL D-TYPE TRANSPARENT LATCHES
WITH 3-STATE OUTPUTS

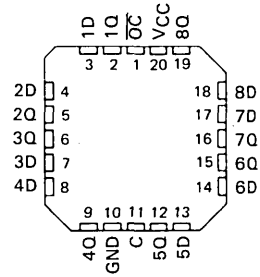
D2684, DECEMBER 1982

- **8 High-Current Latches in a Single Package**
- **High-Current 3-State True Outputs Can Drive up to 15 LSTTL Loads**
- **Full Parallel Access for Loading**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC373 . . . J PACKAGE
SN74HC373 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC373 . . . FH OR FK PACKAGE
SN74HC373 . . . FH OR FN PACKAGE
(TOP VIEW)



description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'HC373 are transparent D-type latches. While the enable (C) is high the Q outputs will follow the data (D) inputs. When the enable is taken low, the Q outputs will be latched at the levels that were set up at the D inputs.

An output-control input ($\overline{OC}$) can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

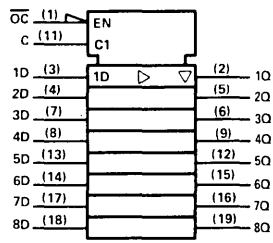
The output control $\overline{OC}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN54HC373 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC373 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE (EACH LATCH)

INPUTS			OUTPUT
$\overline{OC}$	ENABLE C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table III, page 2-5.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

timing requirements (supplement to recommended operating conditions)

		SN54HC373			SN74HC373			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
t_w	Pulse duration, enable C high							ns
t_{su}	Setup time, data before enable C↓							ns
t_h	Hold time, data after enable C↓							ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 45 pF, R_L = 667Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, See Note 1						UNIT
						T_A = 25°C			SN54HC373		SN74HC373	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q											ns
t_{PHL}													
t_{PLH}	C	Any Q											ns
t_{PHL}													
t_{PZH}	OC	Any Q											ns
t_{PZL}													
t_{PHZ}	OC	Any Q											ns
t_{PLZ}													

C_{pd}	Power dissipation capacitance per latch	No load, T_A = 25°C	pF typ

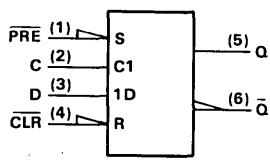
NOTE 1: For load circuit and voltage waveforms, see page 1-14.

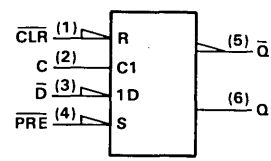
3

D latch signal conventions

It is TI practice to name the outputs and other inputs of a D-type latch and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset; an input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear. Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active-low.

In some applications it may be advantageous to redesignate the data input $\overline{D}$. In that case all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.





Notice that Q and $\overline{Q}$ exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators (▷) on $\overline{PRE}$ and $\overline{CLR}$ remain since these inputs are still active-low, but that the presence or absence of the polarity indicator changes at $\overline{D}$, Q, and $\overline{Q}$. Of course pin 5 ($\overline{Q}$) is still in phase with the data input $\overline{D}$, but now both are considered active-low.

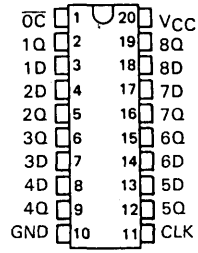
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TYPES SN54HC374, SN74HC374
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS
WITH 3-STATE OUTPUTS

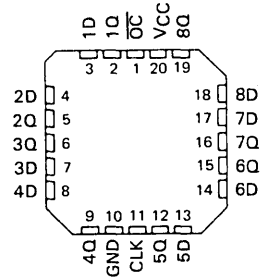
D2684, DECEMBER 1982

- **8 D-Type Flip-Flops in a Single Package**
- **High-Current 3-State True Outputs Can Drive up to 15 LSTTL Loads**
- **Full Parallel Access for Loading**
- **Package Options Include Both Plastic and Ceramic *Chip Carriers in Addition to Plastic and Ceramic* DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC374 . . . J PACKAGE
SN74HC374 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC374 . . . FH OR FK PACKAGE
SN74HC374 . . . FH OR FN PACKAGE
(TOP VIEW)



description

These 8-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the 'HC374 are edge-triggered D-type flip-flops. On the positive transition of the clock the Q outputs will be set to the logic levels that were set up at the D inputs.

An output-control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

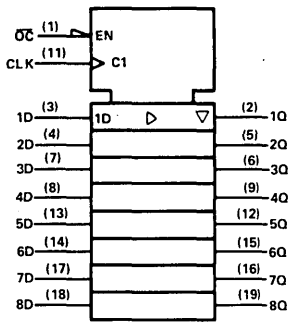
The output control (OC) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54HC374 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74HC374 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table III, page 2-5.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

timing requirements (supplement to recommended operating conditions)

			SN54HC374			SN74HC374			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	CLK high							ns
		CLK low							
t_{su}	Setup time, data before CLK↑								ns
t_h	Hold time, data after CLK↑								ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 45 pF, R_L = 667Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, See Note 1				UNIT
						T_A = 25°C		SN54HC374	SN74HC374	
			MIN	TYP	MAX	MIN	TYP MAX	MIN MAX	MIN MAX	
f_{max}										MHz
t_{PLH}	CLK	Q								ns
t_{PHL}										
t_{PZH}	$\overline{OC}$	Q								ns
t_{PZL}										
t_{PHZ}	$\overline{OC}$	Q								ns
t_{PLZ}										

C_{pd}	Power dissipation capacitance per flip-flop	No load, T_A = 25°C	pF typ

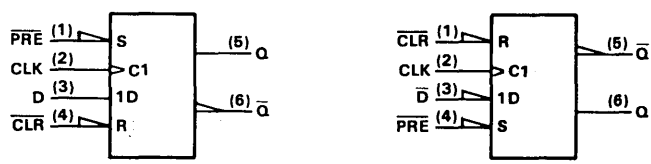
NOTE 1: For load circuit and voltage waveforms, see page 1-14.

3

D flip-flop signal conventions

It is TI practice to name the outputs and other inputs of a D-type flip-flop and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset; an input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear. Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active-low.

In some applications it may be advantageous to redesignate the data input $\overline{D}$. In that case all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.



Notice that Q and $\overline{Q}$ exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators (◺) on $\overline{PRE}$ and $\overline{CLR}$ remain since these inputs are still active-low, but that the presence or absence of the polarity indicator changes at $\overline{D}$, Q, and $\overline{Q}$. Of course pin 5 ($\overline{Q}$) is still in phase with the data input $\overline{D}$, but now both are considered active-low.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TYPES SN54HC377, SN54HC378, SN54HC379 SN74HC377, SN74HC378, SN74HC379 OCTAL, HEX, AND QUAD D-TYPE FLIP-FLOPS WITH ENABLE

D2684, DECEMBER 1982

- **'HC377 and 'HC378 Contain Eight and Six Flip-Flops, Respectively, with Single-Rail Outputs**
- **'HC379 Contains Four Flip-Flops with Double-Rail Outputs**
- **Individual Data Input to Each Flip-Flop**
- **Applications Include:**
  - **Buffer/Storage Registers**
  - **Shift Registers**
  - **Pattern Generators**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These circuits are positive-edge-triggered D-type flip-flops with an enable input. The 'HC377, 'HC378, and 'HC379 devices are similar to 'HC273, 'HC174, and 'HC175 respectively, but feature a common clock enable ($\overline{G}$) instead of a common clear.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if $\overline{G}$ is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output. The circuits are designed to prevent false clocking by transitions at the $\overline{G}$ input.

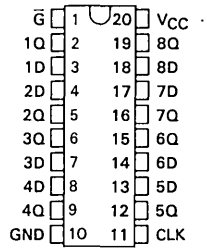
The SN54HC377, SN54HC378, and SN54HC379 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC377, SN74HC378, and SN74HC379 are characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(EACH FLIP-FLOP)

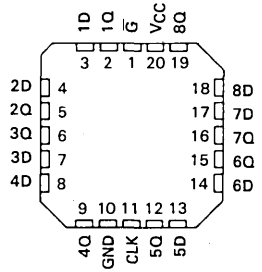
INPUTS			OUTPUTS	
$\overline{G}$	CLOCK	DATA	Q	$\overline{Q}$†
H	X	X	Q_0	$\overline{Q}_0$
L	↑	H	H	L
L	↑	L	L	H
X	L	X	Q_0	$\overline{Q}_0$

†'HC379 only

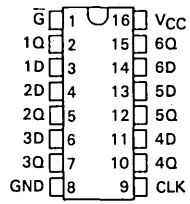
SN54HC377 . . . J PACKAGE
SN74HC377 . . . J OR N PACKAGE
(TOP VIEW)



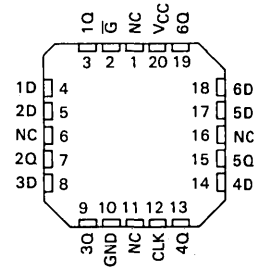
SN54HC377 . . . FH OR FK PACKAGE
SN74HC377 . . . FH OR FN PACKAGE
(TOP VIEW)



SN54HC378 . . . J PACKAGE
SN74HC378 . . . J OR N PACKAGE
(TOP VIEW)

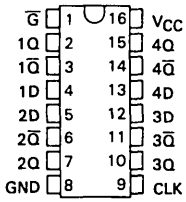


SN54HC378 . . . FH OR FK PACKAGE
SN74HC378 . . . FH OR FN PACKAGE
(TOP VIEW)

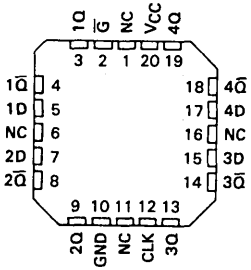


NC — No internal connection

SN54HC379 . . . J PACKAGE
SN74HC379 . . . J OR N PACKAGE
(TOP VIEW)



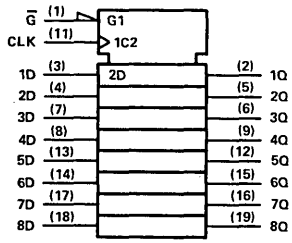
SN54HC379 . . . FH OR FK PACKAGE
SN74HC379 . . . FH OR FN PACKAGE
(TOP VIEW)



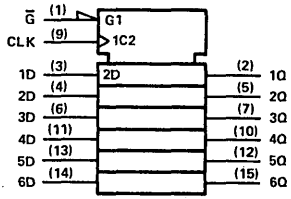
NC — No internal connection

logic symbols

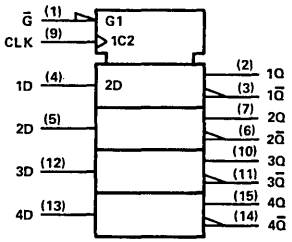
'HC377



'HC378



'HC379



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

'HC377, 'HC378: See Table IV, page 2-6.
'HC379: See Table II, Page 2-4.

timing requirements (supplement to recommended operating conditions)

			SN54HC'			SN74HC'			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration, CLK high or low								ns
t_{su}	Setup time before CLK↑	D							ns
		$\overline{G}$ low							
		$\overline{G}$ high							
t_h	Hold time after CLK↑								ns

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POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF						UNIT
						T_A = 25°C			SN54HC'		SN74HC'	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}													MHz
t_{PLH}	CLK	Any											ns
t_{PHL}													

C_{pd}	Power dissipation capacitance per flip-flop	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

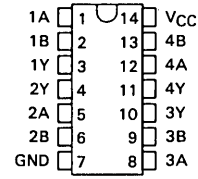
3

TYPES SN54HC386, SN74HC386
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

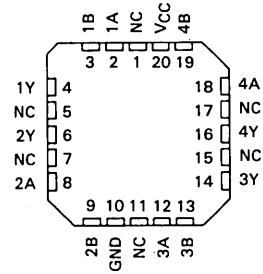
D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC386 . . . J PACKAGE
SN74HC386 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC386 . . . FH OR FK PACKAGE
SN74HC386 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

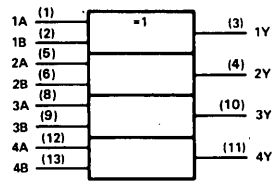
description

These devices contain four independent 2-input Exclusive-OR gates. They perform the boolean functions $Y = A \oplus B = \overline{A}B + A\overline{B}$ in positive logic.

A common application is as a true/complement element. If one of the inputs is low, the other input will be reproduced in true form at the output. If one of the inputs is high, the signal on the other input will be reproduced inverted at the output.

The SN54HC386 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC386 is characterized for operation from −40°C to 85°C.

logic symbol



FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table I, page 2-3.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF						UNIT
						T_A = 25°C			SN54HC386		SN74HC386	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B (other input low)	Y											ns
t_{PHL}													
t_{PLH}	A or B (other input high)	Y											ns
t_{PLH}													
C_{pd}	Power dissipation capacitance per gate					No load, T_A = 25°C					pF typ		

NOTE 1: For load circuit and voltage waveforms, see pages 1-14.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TYPES SN54HC390, SN54HC393, SN74HC390, SN74HC393 DUAL 4-BIT DECADE AND BINARY COUNTERS

D2684, DECEMBER 1982

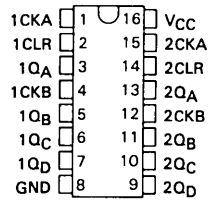
- **'HC390 . . . Individual Clocks for A and B Flip-Flops Provide Dual ÷2 and ÷5 Counters**
- **'HC393 . . . Dual 4-Bit Binary Counter with Individual Clocks**
- **All Have Direct Clear for Each 4-Bit Counter**
- **Dual 4-Bit Versions Can Significantly Improve System Densities by Reducing Counter Package Count by 50%**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

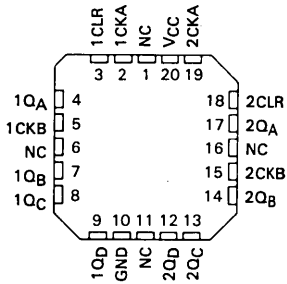
Each of these monolithic circuits contains eight flip-flops and additional gating to implement two individual four-bit counters in a single package. The 'HC390 incorporates dual divide-by-two and divide-by-five counters, which can be used to implement cycle lengths equal to any whole and/or cumulative multiples of 2 and/or 5 up to divide-by-100. When connected as a bi-quinary counter, the separate divide-by-two circuit can be used to provide symmetry (a square wave) at the final output stage. The 'HC393 comprises two independent four-bit binary counters each having a clear and a clock input. N-bit binary counters can be implemented with each package providing the capability of divide-by-256. The 'HC390 and 'HC393 have parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system-timing signals.

The SN54HC390 and SN54HC393 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC390 and SN74HC393 are characterized for operation from −40°C to 85°C.

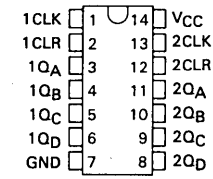
SN54HC390 . . . J PACKAGE
SN74HC390 . . . J OR N PACKAGE
(TOP VIEW)



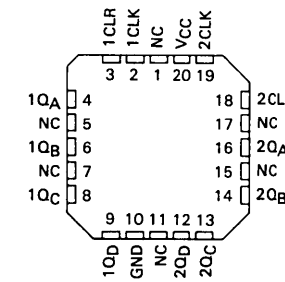
SN54HC390 . . . FH OR FK PACKAGE
SN74HC390 . . . FH OR FN PACKAGE
(TOP VIEW)



SN54HC393 . . . J PACKAGE
SN74HC393 . . . J OR N PACKAGE
(TOP VIEW)



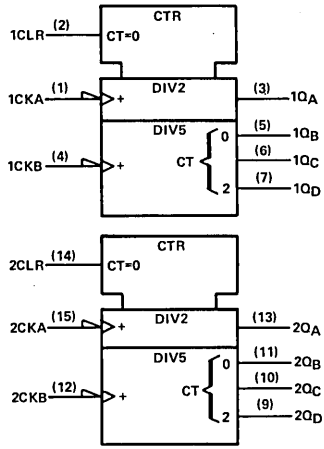
SN54HC393 . . . FH OR FK PACKAGE
SN74HC393 . . . FH OR FN PACKAGE
(TOP VIEW)



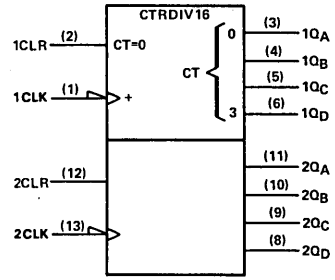
NC — No internal connection

logic symbols

'HC390



'HC393



Pin numbers shown are for J and N packages.

3

FUNCTION TABLES

'HC390
BCD COUNT SEQUENCE
(EACH COUNTER)
(See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

'HC390
BI-QUINARY (5-2)
(EACH COUNTER)
(See Note B)

COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

'HC393
COUNT SEQUENCE
(EACH COUNTER)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTES: A. Output Q_A is connected to input CKB for BCD count.
B. Output Q_D is connected to input CKA for bi-quinary count.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table IV, page 2-6.

TEXAS INSTRUMENTS
INCORPORATED
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timing requirements (supplement to recommended operating conditions)

			SN54HC390 SN54HC393			SN74HC390 SN74HC393			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}	Clock frequency	CKA or CLK							MHz
		CKB							
t_w	Pulse duration	CKA or CLK high or low							ns
		CKB high or low							
		CLR high							
t_{su}	Setup time, clear inactive								ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF					UNIT
						T_A = 25°C			SN54HC'	SN74HC'	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN MAX	MIN MAX	
f_{max}	CKA or CLK	Q_A									MHz
	CKB	Q_B									
t_{PLH}	CKA or CLK	Q_A									ns
t_{PHL}											
t_{PLH}	CKA or CLK	Q_C of 'HC390 Q_D of 'HC393									ns
t_{PHL}											
t_{PLH}	CKB	Q_B									ns
t_{PHL}											
t_{PLH}	CKB	Q_C									ns
t_{PHL}											
t_{PLH}	CKB	Q_D									ns
t_{PHL}											
t_{PHL}	CLR	Any									ns

C_{pd}	Power dissipation capacitance per counter	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

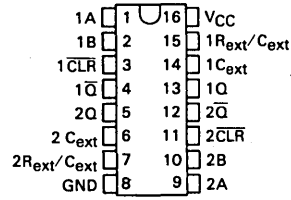
3

TYPES SN54HC423, SN74HC423
DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

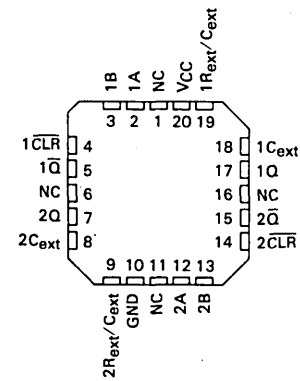
D2684, DECEMBER 1982

- **Retriggerable for Very Long Output Pulses, Up to 100% Duty Cycle**
- **Overriding Clear Terminates Output Pulse**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC423 . . . J PACKAGE
SN74HC423 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC423 . . . FH OR FK PACKAGE
SN74HC423 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

These dc-triggered multivibrators feature output-pulse-duration control by two methods. The basic pulse duration is programmed by selection of external resistance and capacitance values. Once triggered, the basic pulse duration may be extended by retriggering the gated low-level-active (A) or high-level-active (B) inputs, or be reduced by use of the overriding clear. Figure 1 illustrates pulse control by retriggering and early clear.

The B input is a Schmitt trigger enabling jitter-free triggering from input signals with slow transition rates.

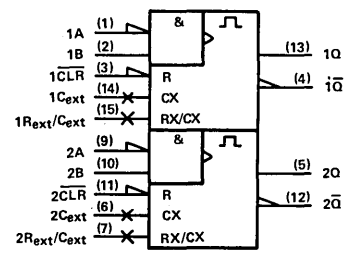
The SN54HC423 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC423 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L*	H*
X	X	L	L*	H*
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎

*These are the logic levels the outputs will take on after the completion of any pulse already started.

logic symbol



Pin numbers shown are for J and N packages.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
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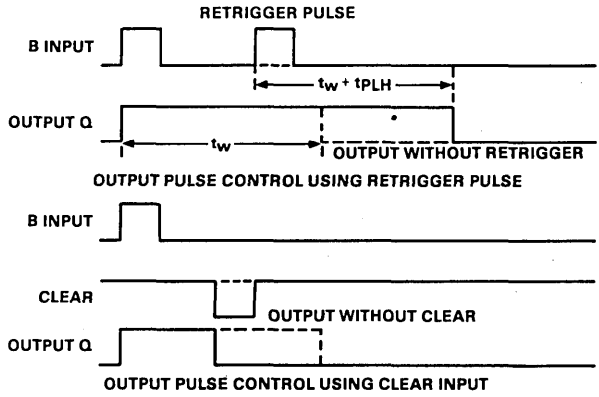


FIGURE 1—TYPICAL INPUT/OUTPUT PULSES

maximum ratings, recommended operating conditions, and electrical characteristics

See Table IV, page 2-6.

Note: The minimum recommended supply voltage for this device is 3 V.

timing requirements (supplement to recommended operating conditions)

		SN54HC423			SN74HC423			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
t_w	Pulse duration, A low, B high, or $\overline{CLR}$ low							ns
C_{ext}	External timing capacitance							μF
R_{ext}	External timing resistance							kΩ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TIMING COMPONENTS		V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C		V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF				UNIT
							T_A = 25°C		SN54HC423	SN74HC423	
			C_{ext}	R_{ext}	MIN	TYP MAX	MIN	TYP MAX	MIN MAX	MIN MAX	
t_{PLH}	A	Q	0	5 kΩ							ns
	B										
t_{PHL}	A	$\overline{Q}$	0	5 kΩ							ns
	B										
t_{PHL}	$\overline{CLR}$	Q	0	5 kΩ							ns
t_{PLH}		$\overline{Q}$									
t_{wQ}(min)	A or B	Q	0	5 kΩ							ns
t_{wQ}			1nF	10 kΩ							μs

C_{pd}	Power dissipation capacitance per multivibrator	No load, T_A = 25°C	pF typ

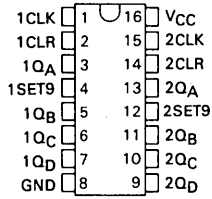
NOTE 1: For load circuit and voltage waveforms, see page 1-14.

TYPES SN54HC490, SN74HC490
DUAL 4-BIT DECADE COUNTERS

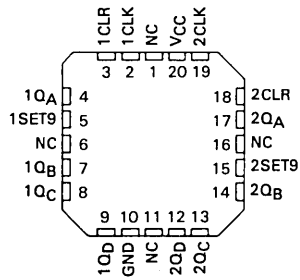
D2684, DECEMBER 1982

- **Individual Clock, Direct Clear, and Set-to-9 Inputs for Each Decade Counter**
- **Dual Counters Can Significantly Improve System Densities as Package Count Can Be Reduced by 50%**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC490 . . . J PACKAGE
SN74HC490 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC490 . . . FH OR FK PACKAGE
SN74HC490 . . . FH OR FN PACKAGE
(TOP VIEW)



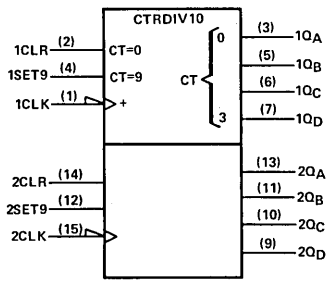
NC — No internal connection

description

Each of these monolithic circuits contains eight master-slave flip-flops and additional gating to implement two individual 4-bit decade counters in a single package. Each decade counter has individual clock, clear, and set-to-9 inputs. BCD count sequences of any length up to divide-by-100 may be implemented with a single 'HC490. The counters have parallel outputs from each counter stage so that submultiples of the input count frequency are available for system timing signals.

The SN54HC490 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC490 is characterized for operation from −40°C to 85°C.

logic symbol



Pin numbers shown are for J and N packages.

CLEAR/SET-TO-9 FUNCTION TABLE (EACH COUNTER)

INPUTS		OUTPUTS			
CLEAR	SET-TO-9	Q_A	Q_B	Q_C	Q_D
H	L	L	L	L	L
L	H	H	L	L	H
L	L	COUNT			

BCD COUNT SEQUENCE (EACH COUNTER)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

maximum ratings, recommended operating conditions, and electrical characteristics

See Table IV, page 2-6.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

timing requirements (supplement to recommended operating conditions)

		SN54HC490			SN74HC490			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}	Clock frequency							MHz
t_w	Pulse duration (any input)							ns
t_{su}	Setup time, clear or set-to-9 inactive							ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF						UNIT
						T_A = 25°C			SN54HC490		SN74HC490	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	MIN	MAX
f_{max}												MHz
t_{PLH}	CLK	Q_A										ns
t_{PHL}												
t_{PLH}	CLK	Q_B, Q_D										ns
t_{PHL}												
t_{PLH}	CLK	Q_C										ns
t_{PHL}												
t_{PHL}	CLR	Any										ns
t_{PLH}	Set-to-9	Q_A, Q_D										ns
t_{PHL}		Q_B, Q_C										

C_{pd}	Power dissipation capacitance per counter	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

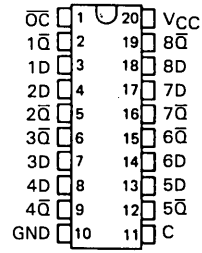
3

TYPES SN54HC533, SN74HC533
OCTAL D-TYPE TRANSPARENT LATCHES
WITH 3-STATE OUTPUTS

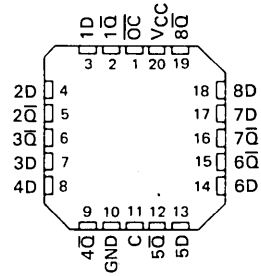
D2684, DECEMBER 1982

- **8 Latches In a Single Package**
- **High-Current 3-State Inverting Outputs Can Drive up to 15 LSTTL Loads**
- **Full Parallel Access for Loading**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC533 . . . J PACKAGE
SN74HC533 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC533 . . . FH OR FK PACKAGE
SN74HC533 . . . FH OR FN PACKAGE
(TOP VIEW)



description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'HC533 are transparent D-type latches. While the enable (C) is high, the $\overline{Q}$ outputs will follow the complements of the D inputs. When the enable is taken low, the $\overline{Q}$ outputs will be latched at the inverses of the levels that were set up at the D inputs. The 'HC533 is functionally equivalent to the 'HC373 except for having inverted outputs.

An output-control ($\overline{OC}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

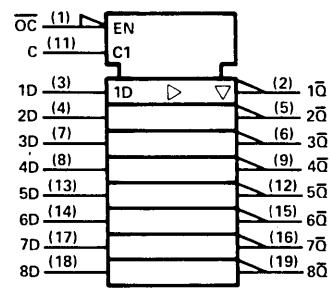
The output control does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN54HC533 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC533 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE (EACH LATCH)

INPUTS			OUTPUT
$\overline{OC}$	ENABLE C	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table III, page 2-5.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

timing requirements (supplement to recommended operating conditions)

		SN54HC533			SN74HC533			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}	Clock frequency							MHz
t_w	Pulse duration, enable C high							ns
t_{su}	Setup time, data before enable C↓							ns
t_h	Hold time, data after enable C↓							ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 45 pF, R_L = 667Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, See Note 1						UNIT
						T_A = 25°C			SN54HC533		SN74HC533	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}													MHz
t_{PLH}	D	$\overline{Q}$											ns
t_{PHL}													
t_{PLH}	C	Any											ns
t_{PHL}													
t_{PZH}	$\overline{OC}$	Any											ns
t_{PZL}													
t_{PHZ}	$\overline{OC}$	Any											ns
t_{PLZ}													

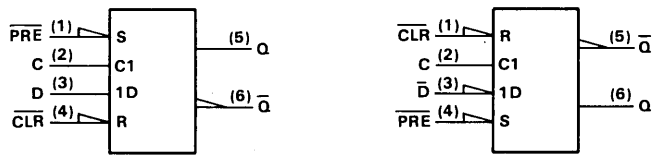
C_{pd}	Power dissipation capacitance per latch	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

D latch signal conventions

It is TI practice to name the outputs and other inputs of a D-type latch and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset; an input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear. Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active-low.

In some applications it may be advantageous to redesignate the data input $\overline{D}$. In that case all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.



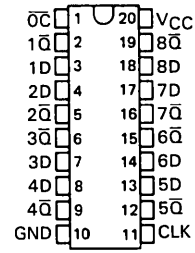
Notice that Q and $\overline{Q}$ exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators (▷) on $\overline{PRE}$ and $\overline{CLR}$ remain since these inputs are still active-low, but that the presence or absence of the polarity indicator changes at $\overline{D}$, Q, and $\overline{Q}$. Of course pin 5 ($\overline{Q}$) is still in phase with the data input $\overline{D}$, but now both are considered active-low.

TYPES SN54HC534, SN74HC534
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS
WITH 3-STATE OUTPUTS

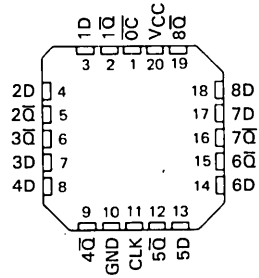
D2684, DECEMBER 1982

- **High-Current 3-State Inverting Outputs Can Drive up to 15 LSTTL Loads**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC534 . . . J PACKAGE
SN74HC534 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC534 . . . FH OR FK PACKAGE
SN74HC534 . . . FH OR FN PACKAGE
(TOP VIEW)



description

These 8-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low impedance loads. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

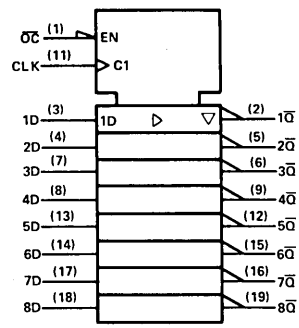
The eight flip-flops of the 'HC534 are edge-triggered D-type flip-flops. On the positive transition of the clock, the $\overline{Q}$ outputs will be set to the complement of the logic states that were set up at the D inputs. The 'HC534 is functionally equivalent to the 'HC374 except for having inverted outputs.

An output-control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

The SN54HC534 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74HC534 is characterized for operation from -40°C to 85°C.

logic symbol



Pin numbers shown are for J and N packages.

FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

maximum ratings, recommended operating conditions, and electrical characteristics

See Table III, page 2-5.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

timing requirements (supplement to recommended operating conditions)

			SN54HC534			SN74HC534			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	CLK high							ns
		CLK low							
t_{su}	Setup time, data before CLK↑								ns
t_h	Hold time, data after CLK↑								ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 45 pF, R_L = 667Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, See Note 1					UNIT
						T_A = 25°C			SN54HC534	SN74HC534	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN MAX	MIN MAX	
f_{max}											MHz
t_{PLH}	CLK	Any									ns
t_{PHL}											
t_{PZH}	$\overline{OC}$	Any									ns
t_{PZL}											
t_{PHZ}	$\overline{OC}$	Any									ns
t_{PLZ}											

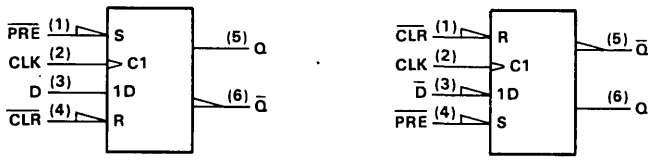
C_{pd}	Power dissipation capacitance per flip-flop	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

D flip-flop signal conventions

It is TI practice to name the outputs and other inputs of a D-type flip-flop and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset; an input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear. Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active-low.

In some applications it may be advantageous to redesignate the data input $\overline{D}$. In that case all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.



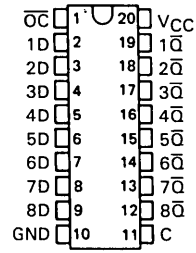
Notice that Q and $\overline{Q}$ exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators (▷) on $\overline{PRE}$ and $\overline{CLR}$ remain since these inputs are still active-low, but that the presence or absence of the polarity indicator changes at $\overline{D}$, Q, and $\overline{Q}$. Of course pin 5 ($\overline{Q}$) is still in phase with the data input $\overline{D}$, but now both are considered active-low.

TYPES SN54HC563, SN74HC563
OCTAL D-TYPE TRANSPARENT LATCHES
WITH 3-STATE OUTPUTS

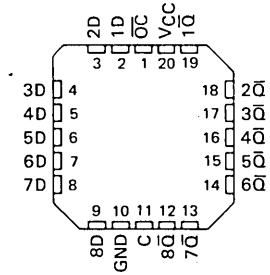
D2684, DECEMBER 1982

- **High-Current 3-State Outputs Drive Bus-Lines Directly or up to 15 LSTTL Loads**
- **Bus-Structured Pinout**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC563 . . . J PACKAGE
SN74HC563 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC563 . . . FH OR FK PACKAGE
SN74HC563 . . . FH OR FN PACKAGE
(TOP VIEW)



description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches are transparent D-type latches. While the enable (C) is high the $\overline{Q}$ outputs will follow the complements of data (D) inputs. When the enable is taken low the outputs will be latched at the inverses of the levels that were set up at the D inputs.

An output-control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased high-logic level provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

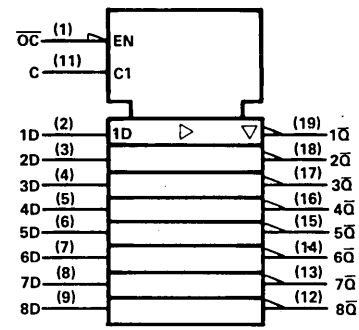
The output control ($\overline{OC}$) does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54HC563 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC563 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(Each Latch)

INPUTS			OUTPUT
ENABLE			
$\overline{OC}$	C	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	Q_0
H	X	X	Z

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table III, page 2-5.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

timing requirements (supplement to recommended operating conditions)

		SN54HC563			SN74HC563			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
t_w	Pulse duration, enable C high							ns
t_{su}	Setup time, data before enable C↑							ns
t_h	Hold time, data after enable C↑							ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 45 pF, R_L = 667Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, See Note 1					UNIT
						T_A = 25°C			SN54HC563	SN74HC563	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN MAX	MIN MAX	
t_{PLH}	D	$\overline{Q}$									ns
t_{PHL}											
t_{PLH}	C	Any									ns
t_{PHL}											
t_{PZH}	$\overline{OC}$	Any									ns
t_{PZL}											
t_{PHZ}	$\overline{OC}$	Any									ns
t_{PLZ}											

C_{pd}	Power dissipation capacitance per latch	No load, T_A = 25°C	pF typ

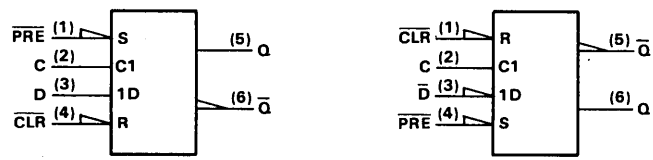
NOTE 1: For load circuit and voltage waveforms, see page 1-14.

3

D latch signal conventions

It is TI practice to name the outputs and other inputs of a D-type latch and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset; an input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear. Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active-low.

In some applications it may be advantageous to redesignate the data input $\overline{D}$. In that case all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.



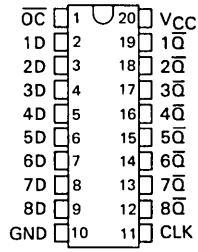
Notice that Q and $\overline{Q}$ exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators (▷) on $\overline{PRE}$ and $\overline{CLR}$ remain since these inputs are still active-low, but that the presence or absence of the polarity indicator changes at $\overline{D}$, Q, and $\overline{Q}$. Of course pin 5 ($\overline{Q}$) is still in phase with the data input $\overline{D}$, but now both are considered active-low.

TYPES SN54HC564, SN74HC564
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

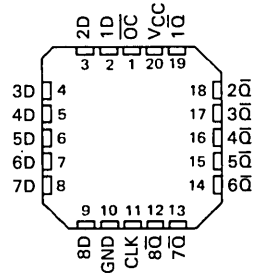
D2684, DECEMBER 1982

- **High-Current 3-State Inverting Outputs Drive Bus-Lines Directly or up to 15 LSTTL Loads**
- **Bus-Structured Pinout**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC564 . . . J PACKAGE
SN74HC564 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC564 . . . FH OR FK PACKAGE
SN74HC564 . . . FH OR FN PACKAGE
(TOP VIEW)



description

These 8-bit registers feature inverting three-state outputs designed specifically for bus driving. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight-bit edge-triggered D-type flip-flops enter data on the low-to-high transition of the clock.

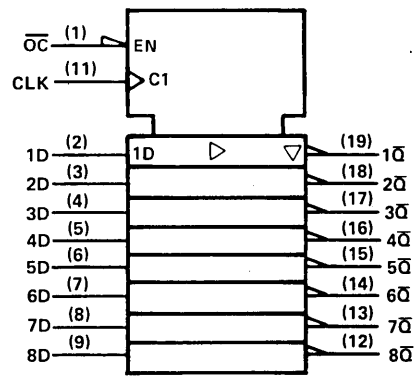
The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54HC564 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC564 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table III, page 2-5.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

timing requirements (supplement to recommended operating conditions)

			SN54HC564			SN74HC564			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	CLK high							ns
		CLK low							
t_{su}	Setup time, data before CLK↑								ns
t_h	Hold time, data after CLK↑								ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 45 pF, R_L = 667Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, See Note 1						UNIT
						T_A = 25°C			SN54HC564		SN74HC564	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	MIN	MAX
f_{max}												MHz
t_{PLH}	CLK	Any										ns
t_{PHL}												
t_{PZH}	$\overline{OC}$	Any										ns
t_{PZL}												
t_{PHZ}	$\overline{OC}$	Any										ns
t_{PLZ}												

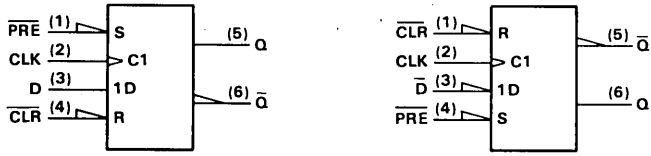
C_{pd}	Power dissipation capacitance per flip-flop	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

D flip-flop signal conventions

It is TI practice to name the outputs and other inputs of a D-type flip-flop and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset; an input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear. Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active-low.

In some applications it may be advantageous to redesignate the data input $\overline{D}$. In that case all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.



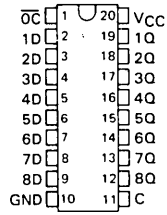
Notice that Q and $\overline{Q}$ exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators (▷) on $\overline{PRE}$ and $\overline{CLR}$ remain since these inputs are still active-low, but that the presence or absence of the polarity indicator changes at $\overline{D}$, Q, and $\overline{Q}$. Of course pin 5 ($\overline{Q}$) is still in phase with the data input $\overline{D}$, but now both are considered active-low.

TYPES SN54HC573, SN74HC573
OCTAL D-TYPE TRANSPARENT LATCHES
WITH 3-STATE OUTPUTS

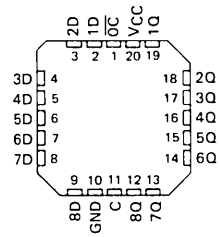
D2684, DECEMBER 1982

- **High-Current 3-State Outputs Drive Bus-Lines Directly or up to 15 LSTTL Loads**
- **Bus-Structured Pinout**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC573 . . . J PACKAGE
SN74HC573 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC573 . . . FH OR FK PACKAGE
SN74HC573 . . . FH OR FN PACKAGE
(TOP VIEW)



description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches are transparent D-type latches. While the enable (C) is high the outputs (Q) will respond to the data (D) inputs. When the enable is taken low the outputs will be latched to retain the data that was set up.

An output-control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

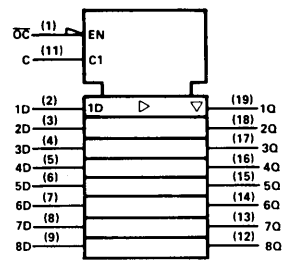
The output control ($\overline{OC}$) does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are at high impedance.

The SN54HC573 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74HC573 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE
(EACH LATCH)

INPUTS			OUTPUT
ENABLE			Q
$\overline{OC}$	C	D	
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table III, page 2-5.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

timing requirements (supplement to recommended operating conditions)

		SN54HC573			SN74HC573			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
t_w	Pulse duration, C high							ns
t_{su}	Setup time, data before enable C↑							ns
t_h	Hold time, data after enable C↑							ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 45 pF, R_L = 667Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, See Note 1						UNIT
						T_A = 25°C			SN54HC573		SN74HC573	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	$\overline{Q}$											ns
t_{PHL}													
t_{PLH}	C	Any											ns
t_{PHL}													
t_{PZH}	$\overline{OC}$	Any											ns
t_{PZL}													
t_{PHZ}	$\overline{OC}$	Any											ns
t_{PLZ}													

C_{pd}	Power dissipation capacitance per latch	No load, T_A = 25°C	pF typ

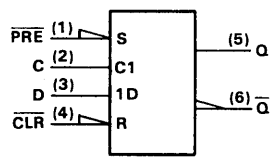
NOTE 1: For load circuit and voltage waveforms, see page 1-14.

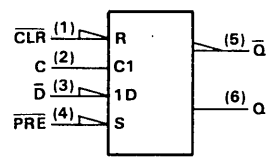
3

D latch signal conventions

It is TI practice to name the outputs and other inputs of a D-type latch and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset; an input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear. Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active-low.

In some applications it may be advantageous to redesignate the data input $\overline{D}$. In that case all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.





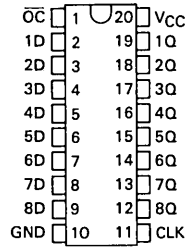
Notice that Q and $\overline{Q}$ exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators (▷) on $\overline{PRE}$ and $\overline{CLR}$ remain since these inputs are still active-low, but that the presence or absence of the polarity indicator changes at $\overline{D}$, Q, and $\overline{Q}$. Of course pin 5 ($\overline{Q}$) is still in phase with the data input $\overline{D}$, but now both are considered active-low.

TYPES SN54HC574, SN74HC574
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

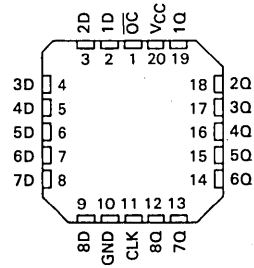
D2684, DECEMBER 1982

- **High-Current 3-State Noninverting Outputs Drive Bus-Lines Directly or up to 15 LSTTL Loads**
- **Bus-Structured Pinout**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC574 . . . J PACKAGE
SN74HC574 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC574 . . . FH OR FK PACKAGE
SN74HC574 . . . FH OR FN PACKAGE
(TOP VIEW)



description

These 8-bit registers feature three-state outputs designed specifically for bus driving. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight edge-triggered D-type flip-flops enter data on the low-to-high transition of the clock.

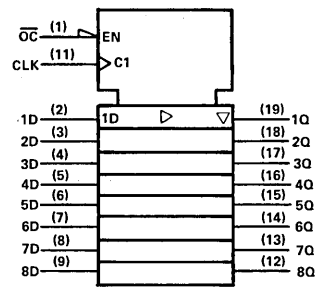
The output-control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54HC574 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC574 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table III, page 2-5.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

timing requirements (supplement to recommended operating conditions)

			SN54HC574			SN74HC574			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	CLK high							ns
		CLK low							
t_{su}	Setup time, data before CLK↑								ns
t_h	Hold time, data after CLK↑								ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 45 pF, R_L = 667Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, See Note 1					UNIT
						T_A = 25°C			SN54HC574	SN74HC574	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN MAX	MIN MAX	
f_{max}											MHz
t_{PLH}	CLK	Any									ns
t_{PHL}											
t_{PZH}	$\overline{OC}$	Any									ns
t_{PZL}											
t_{PHZ}	$\overline{OC}$	Any									ns
t_{PLZ}											

C_{pd}	Power dissipation capacitance per flip-flop	No load, T_A = 25°C	pF typ

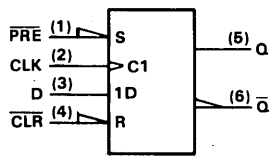
Note: 1. For load circuit and voltage waveforms, see page 1-14.

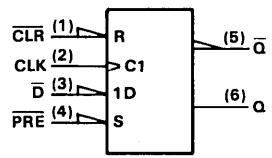
3

D flip-flop signal conventions

It is TI practice to name the outputs and other inputs of a D-type flip-flop and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset; an input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear. Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active-low.

In some applications it may be advantageous to redesignate the data input $\overline{D}$. In that case all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.

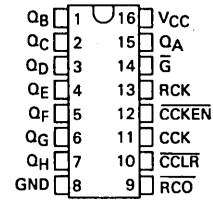




Notice that Q and $\overline{Q}$ exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators (◺) on $\overline{PRE}$ and $\overline{CLR}$ remain since these inputs are still active-low, but that the presence or absence of the polarity indicator changes at $\overline{D}$, Q, and $\overline{Q}$. Of course pin 5 ($\overline{Q}$) is still in phase with the data input $\overline{D}$, but now both are considered active-low.

- 8-Bit Counter with Register
- High-Current 3-State Parallel Register Outputs Can Drive up to 15 LSTTL Loads
- Counter Has Direct Clear
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54HC590 . . . J PACKAGE
SN74HC590 . . . J OR N PACKAGE
(TOP VIEW)



For chip carrier information, contact the factory

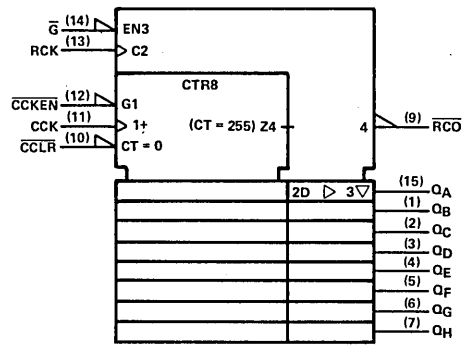
description

These devices each contain an 8-bit binary counter that feeds an 8-bit storage register. The storage register has parallel outputs. Separate clocks are provided for both the binary counter and storage register. The binary counter features a direct clear input $\overline{CCLR}$ and a count enable input $\overline{CCKEN}$. For cascading a ripple carry output $\overline{RCO}$ is provided. Expansion is easily accomplished by tying $\overline{RCO}$ of the first stage to $\overline{CCKEN}$ of the second stage, etc.

Both the counter and register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the counter state will always be one count ahead of the register. Internal circuitry prevents clocking from the clock enable.

The SN54HC590 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC590 is characterized for operation from −40°C to 85°C.

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table III, page 2-5.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
INCORPORATED
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timing requirements (supplement to recommended operating conditions)

			SN54HC590			SN74HC590			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}	Clock frequency, CCK or RCK								MHz
t_w	Pulse duration	CCK or RCK high or low							ns
		$\overline{CCLR}$ low							
t_{su}	Setup time	$\overline{CCKEN}$ low before CCK↑							ns
		$\overline{CCLR}$ high (inactive) before CCK↑							
		CCK↑ before RCK↑†							

†This setup time ensures the register will see stable data from the counter outputs. The clocks may be tied together in which case the register state will be one clock pulse behind the counter.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = Note 2, R_L = Note 2, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF					UNIT
						T_A = 25°C			SN54HC590	SN74HC590	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN MAX	MIN MAX	
f_{max}	CCK or RCK										MHz
t_{PLH}	CCK↑	$\overline{RCO}$									ns
t_{PHL}											
t_{PLH}	$\overline{CCLR}$↓	$\overline{RCO}$									ns
t_{PLH}	RCK↑	Q									ns
t_{PHL}											
t_{PZH}	$\overline{G}$↓	Q									ns
t_{PZL}											
t_{PHZ}	$\overline{G}$↑	Q									ns
t_{PLZ}											

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	pF typ

NOTES: 1. For load circuit and voltage waveforms, see page 1-14.
2. C_L = 15 pF and R_L = 2 kΩ for RCO output;
C_L = 45 pF and R_L = 667Ω for Q outputs.

TYPES SN54HC592, SN54HC593, SN74HC592, SN74HC593 8-BIT BINARY COUNTERS WITH INPUT REGISTERS

D2684, DECEMBER 1982

- Parallel Register Inputs ('HC592)
- Parallel 3-State I/O: Register Inputs/Counter Outputs ('HC593)
- Counter Has Direct Overriding Load and Clear
- High-Current Outputs Can Drive up to 15 LSTTL Loads ('HC593)
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

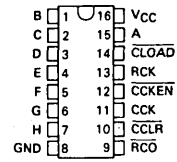
description

The 'HC592 consists of a parallel input, 8-bit storage register feeding an 8-bit binary counter. Both the register and the counter have individual positive edge-triggered clocks. In addition, the counter has direct load and clear functions. Expansion is easily accomplished by connecting $\overline{RCO}$ of the first stage to the count enable of the second stage, etc.

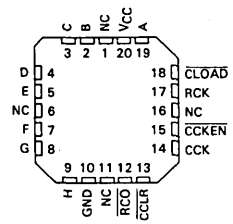
The 'HC593 has all the features of the 'HC592 plus 3-state I/O, which provides parallel counter outputs.

The SN54HC592 and SN54HC593 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC592 and SN74HC593 are characterized for operation from −40°C to 85°C.

SN54HC592 . . . J PACKAGE
SN74HC592 . . . J OR N PACKAGE
(TOP VIEW)

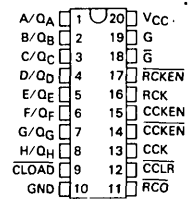


SN54HC592 . . . FH OR FK PACKAGE
SN74HC592 . . . FH OR FN PACKAGE
(TOP VIEW)

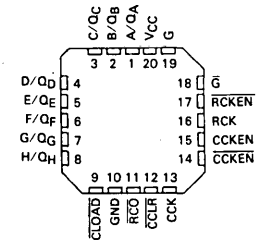


NC — No internal connection

SN54HC593 . . . J PACKAGE
SN74HC593 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC593 . . . FH OR FK PACKAGE
SN74HC593 . . . FH OR FN PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
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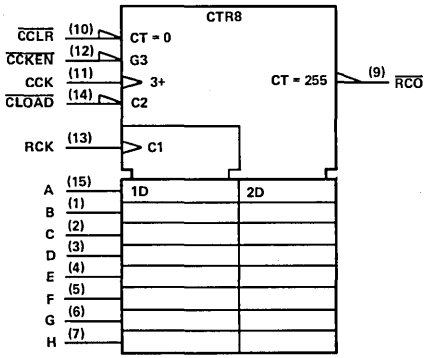
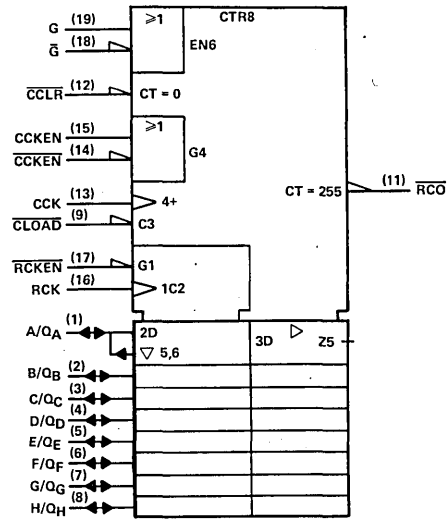
logic symbols

'HC592



'HC593



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

'HC592: See Table IV,page 2-6.
'HC593: See Table III, page 2-5.

timing requirements (supplement to recommended operating conditions)

			SN54HC'			SN74HC'			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}	Clock frequency, CCK or RCK								MHz
t_w	Pulse duration	CCK or RCK high or low							ns
		$\overline{CCLR}$ low							
		$\overline{CLOAD}$ low							
t_{su}	Setup time (see Note)	$\overline{CCKEN}$ low before CCK							ns
		$\overline{CCLR}$ high (inactive) before CCK↑							
		RCK↑ before CCK↑							
		Data A thru H before RCK↑							
t_h	Hold time								ns

NOTE: The RCK↑ to CCK↑ setup time ensures the counter will see stable data from the register outputs.

'HC592 switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF				UNIT
						T_A = 25°C		SN54HC592	SN74HC592	
			MIN	TYP	MAX	MIN	TYP MAX	MIN MAX	MIN MAX	
f_{max}	CCK or RCK									MHz
t_{PLH}	CCK↑	$\overline{RCO}$								ns
t_{PHL}										
t_{PLH}	$\overline{CLOAD}$↓	$\overline{RCO}$								ns
t_{PHL}										
t_{PLH}	$\overline{CCLR}$↓	$\overline{RCO}$								ns
t_{PLH}	RCK↑	$\overline{RCO}$								ns
t_{PHL}										

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

3

'HC593 switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 45 pF, R_L = 667Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, See Note 1				UNIT
						T_A = 25°C		SN54HC593	SN74HC593	
			MIN	TYP	MAX	MIN	TYP MAX	MIN MAX	MIN MAX	
f_{max}	CCK or RCK									MHz
t_{PLH}	CCK↑	Q								ns
t_{PHL}										
t_{PLH}	$\overline{CLOAD}$↓	Q								ns
t_{PHL}										
t_{PHL}	$\overline{CCLR}$↓	Q								ns
t_{PZH}	G↑	Q								ns
t_{PZL}										
t_{PZH}	$\overline{G}$↓	Q								ns
t_{PZL}										
t_{PHZ}	G↓	Q								ns
t_{PLZ}										
t_{PHZ}	$\overline{G}$↑	Q								ns
t_{PLZ}										
t_{PLH}	CCK↑	$\overline{RCO}$								ns
t_{PHL}										
t_{PLH}	$\overline{CLOAD}$↓	$\overline{RCO}$								ns
t_{PHL}										
t_{PLH}	$\overline{CCLR}$↓	$\overline{RCO}$								ns
t_{PLH}	RCK↑	$\overline{RCO}$								ns
t_{PHL}										

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

TEXAS INSTRUMENTS
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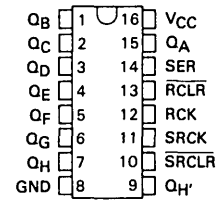
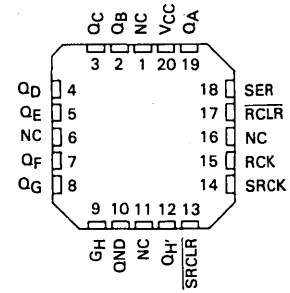
TYPES SN54HC594, SN74HC594 8-BIT SHIFT REGISTERS WITH OUTPUT REGISTERS

- 8-Bit Serial-In, Parallel-Out Shift Registers With Storage
- Independent Direct-Overriding Clears On Shift And Storage Registers
- Independent Clocks for Both Shift and Storage Registers
- High-Current Outputs Can Drive up to 15 LSTTL Loads
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54HC594 . . . J PACKAGE
SN74HC594 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC594 . . . FH OR FK PACKAGE
SN74HC594 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

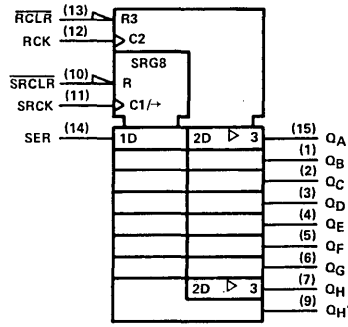
These devices each contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clocks and direct-overriding clears are provided on both the shift and storage registers. A serial output ($Q_{H'}$) is provided for cascading purposes.

Both the shift register and storage register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the shift register will always be one clock pulse ahead of the storage register.

The parallel outputs (Q_A thru Q_H) have high-current capability; output $Q_{H'}$ is a standard output.

The SN54HC594 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74HC594 is characterized for operation from -40°C to 85°C.

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table III, page 2-5.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
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POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

timing requirements (supplement to recommended operating conditions)

			SN54HC594			SN74HC594			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}	Clock frequency, RCK or SRCK								MHz
t_w	Pulse duration	RCK or SRCK high or low							ns
		$\overline{SRCLR}$ low							
t_{su}	Setup time	$\overline{SRCLR}$ high (inactive) before SRCK↑							ns
		$\overline{RCLR}$ high (inactive) before RCK↑							
		SER data before SRCK↑							
		SRCK↑ before RCK↑ (see note)							
t_h	Hold time	SER after SRCK↑							ns

NOTE: This setup time ensures the register will see stable data from the shift-register outputs. The clocks may be connected together in which case the storage register state will be one clock pulse behind the shift register.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, See Note 1					UNIT
						T_A = 25°C			SN54HC594	SN74HC594	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN MAX	MIN MAX	
f_{max}	RCK or SRCK										MHz
t_{PLH}	SRCK	$Q_{H'}$									ns
t_{PHL}											
t_{PLH}	RCK	Q_A thru Q_H									ns
t_{PHL}											
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$									ns
	$\overline{RCLR}$	Q_A thru Q_H									

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

TEXAS INSTRUMENTS
INCORPORATED
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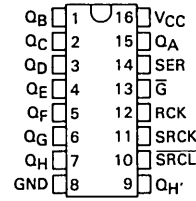
TYPES SN54HC595, SN74HC595
8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUT REGISTERS

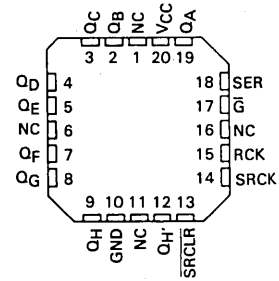
D2684, DECEMBER 1982

- **8-Bit Serial-In, Parallel-Out Shift Registers with Storage**
- **High-Current 3-State Outputs Can Drive up to 15 LSTTL Loads**
- **Shift Register Has Direct Clear**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC595 . . . J PACKAGE
SN74HC595 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC595 . . . FH OR FK PACKAGE
SN74HC595 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

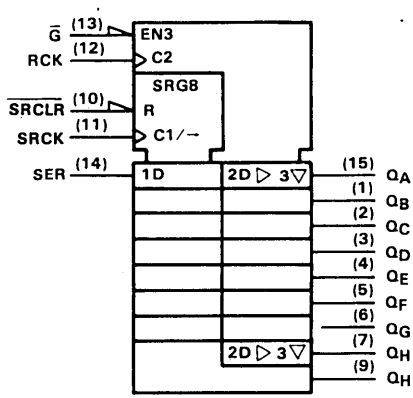
description

These devices each contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct-overriding clear, serial input, and serial output pins for cascading.

Both the shift register and storage register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the shift register state will always be one clock pulse ahead of the storage register.

The SN54HC595 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC595 is characterized for operation from −40°C to 85°C.

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table III, page 2-5.

timing requirements (supplement to recommended operating conditions)

			SN54HC595			SN74HC595			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}	Clock frequency, RCK or SRCK								MHz
t_w	Pulse duration	RCK or SRCK high or low							ns
		$\overline{\text{SRCLR}}$ low							
t_{su}	Setup time	$\overline{\text{SRCLR}}$ high (inactive) before SRCK↑							ns
		SER data before SRCK↑							
		SRCK↑ before RCK↑†							
t_h	Hold time	SER data after SRCK↑							ns

†This setup time ensures the register will see stable data from the shift-register outputs. The clocks may be connected together in which case the storage register state will be one clock pulse behind the shift register.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = Note 2, R_L = Note 2, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, See Note 1					UNIT
						T_A = 25°C			SN54HC595	SN74HC595	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN MAX	MIN MAX	
f_{max}	RCK or SRCK										MHZ
t_{PLH}	SRCK	Q_H'									ns
t_{PHL}											
t_{PHL}	$\overline{\text{SRCLR}}$	Q_H'									ns
t_{PLH}	RCK	Q_A thru Q_H									ns
t_{PHL}											
t_{PZH}	$\overline{G}$	Q_A thru Q_H									ns
t_{PZL}											
t_{PHZ}	$\overline{G}$	Q_A thru Q_H									ns
t_{PLZ}											

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	pF typ

NOTES: 1. For load circuit and voltage waveforms, see page 1-14.
2. C_L = 15 pF and R_L = 2 kΩ for Q_H' output;
C_L = 45 pF and R_L = 667Ω for Q_A thru Q_H outputs.

TEXAS INSTRUMENTS
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TYPES SN54HC597, SN54HC598, SN74HC597, SN74HC598 8-BIT SHIFT REGISTERS WITH INPUT LATCHES

D2684, DECEMBER 1982

- 8-Bit Parallel Storage Register Inputs ('HC597)
- Parallel 3-State I/O, Storage Register Inputs, Shift Register Outputs ('HC598)
- High-Current 3-State Outputs Can Drive up to 15 LSTTL Loads ('HC598)
- Shift Register Has Direct Overriding Load and Clear
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

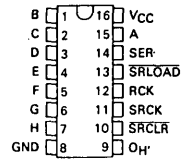
description

The 'HC597 consists of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and shift register have positive-edge triggered clocks. The shift register also has direct load (from storage) and clear inputs.

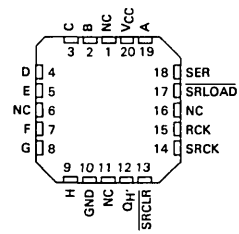
The 'HC598 has all the features of the 'HC597 plus 3-state I/O ports that provide parallel shift register outputs. The 'HC598 also has multiplexed serial data inputs.

The SN54HC597 and SN54HC598 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC597 and SN74HC598 are characterized for operation from −40°C to 85°C.

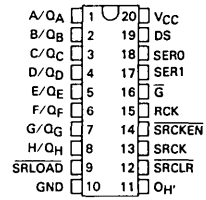
SN54HC597 . . . J PACKAGE
SN74HC597 . . . J OR N PACKAGE
(TOP VIEW)



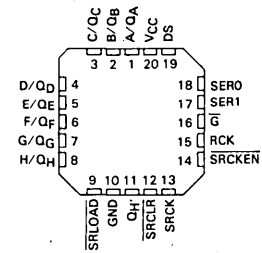
SN54HC597 . . . FH OR FK PACKAGE
SN74HC597 . . . FH OR FN PACKAGE
(TOP VIEW)



SN54HC598 . . . J PACKAGE
SN74HC598 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC598 . . . FH OR FK PACKAGE
SN74HC598 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
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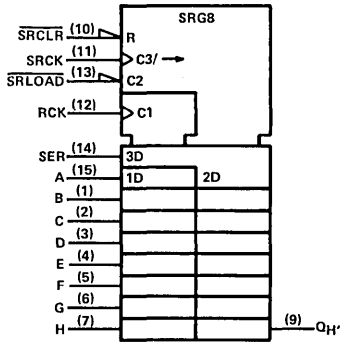
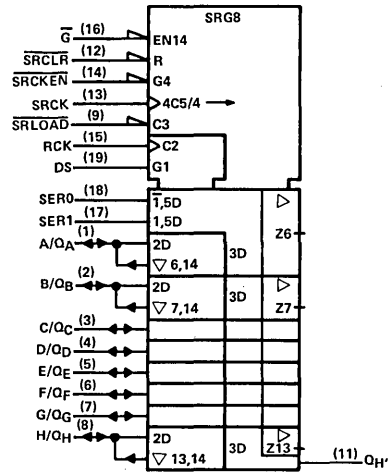
logic symbols

'HC597



'HC598



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

'HC597: See Table IV, page 2-6.
'HC598: See Table III, page 2-5.

timing requirements (supplement to recommended operating conditions)

			SN54HC'			SN74HC'			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}	Clock frequency, RCK or SRCK								MHz
t_w	Pulse duration	RCK or SRCK high or low							ns
		$\overline{SRCLR}$ low							
		$\overline{SRLOAD}$ low							
t_{su}	Setup time (see Note)	$\overline{SRCKEN}$ low before SRCK↑							ns
		$\overline{SRCLR}$ high (inactive) before SRCK↑							
		RCK↑ before SRCK↑							
		SER data before SRCK↑							
		Data A thru H before RCK↑							
t_h	Hold time								ns

NOTE: The RCK ↑ before SRCK↑ setup time ensures that the shift register will see stable data coming from the input register.

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'HC597 switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF				UNIT
						T_A = 25°C		SN54HC597	SN74HC597	
			MIN	TYP	MAX	MIN	TYP MAX	MIN MAX	MIN MAX	
f_{max}	RCK or SRCK									MHz
t_{PLH}	SRCK↑	$Q_{H'}$								ns
t_{PHL}										
t_{PLH}	$\overline{SRLOAD}$↓	$Q_{H'}$								ns
t_{PHL}										
t_{PHL}	$\overline{SCLR}$↓	$Q_{H'}$								ns
t_{PLH}	RCK↑	$Q_{H'}$								ns
t_{PHL}										

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

'HC598 switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = Note 2, R_L = Note 2, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, See Note 1				UNIT
						T_A = 25°C		SN54HC598	SN74HC598	
			MIN	TYP	MAX	MIN	TYP MAX	MIN MAX	MIN MAX	
f_{max}	RCK or SRCK									MHz
t_{PLH}	SRCK↑	$Q_{H'}$								ns
t_{PHL}										
t_{PLH}	$\overline{SRLOAD}$↓	$Q_{H'}$								ns
t_{PHL}										
t_{PHL}	$\overline{SRCLR}$↓	$Q_{H'}$								ns
t_{PLH}	RCK↑	$Q_{H'}$								ns
t_{PHL}										
t_{PLH}	SRCK↑	Q_A thru Q_H								ns
t_{PHL}										
t_{PLH}	$\overline{SRLOAD}$↓	Q_A thru Q_H								ns
t_{PHL}										
t_{PHL}	$\overline{SRCLR}$↓	Q_A thru Q_H								
t_{PZH}	$\overline{G}$↓	Q_A thru Q_H								ns
t_{PZL}										
t_{PHZ}	$\overline{G}$↑	Q_A thru Q_H								ns
t_{PLZ}										

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	pF typ

NOTES: 1. For load circuit and voltage waveforms, see page 1-14.
2. C_L = 15 pF and R_L = 2 kΩ for $Q_{H'}$ output;
C_L = 45 pF and R_L = 667Ω for Q_A through Q_H outputs.

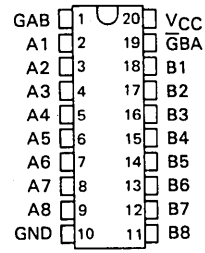
TYPES SN54HC620, SN54HC623, SN74HC620, SN74HC623 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

D2684, DECEMBER 1982

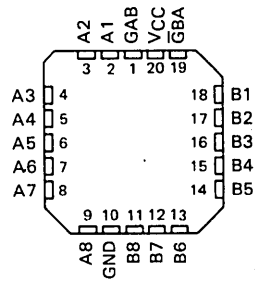
- **Bus Transceivers in High-Density 20-Pin DIPs and also Plastic and Ceramic Chip Carriers**
- **Lock Bus-Latch Capability**
- **Choice of True or Inverting Logic**
- **High-Current 3-State Outputs Can Drive up to 15 LSTTL Loads**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	LOGIC
'HC620	Inverting
'HC623	True

SN54HC'. . . J PACKAGE
SN74HC'. . . J OR N PACKAGE
(TOP VIEW)



SN54HC'. . . FH OR FK PACKAGE
SN74HC'. . . FH OR FN PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ($\overline{G}$BA and GAB).

The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives these devices the capability to store data by simultaneous enabling of $\overline{G}$BA and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical for the 'HC623 or complementary for the 'HC620.

The SN54HC620 and SN54HC623 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC620 and SN74HC623 are characterized for operation from −40°C to 85°C.

FUNCTION TABLE

ENABLE INPUTS		OPERATION	
$\overline{G}$BA	GAB	'HC620	'HC623
L	L	$\overline{B}$ data to A bus	B data to A bus
H	H	$\overline{A}$ data to B bus	A data to B bus
H	L	Isolation	Isolation
L	H	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus	B data to A bus, A data to B bus

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
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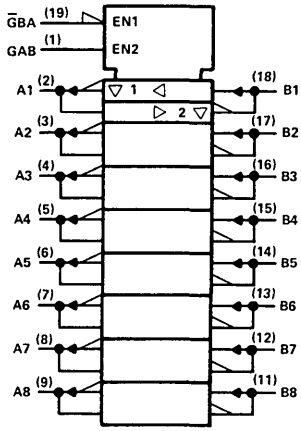
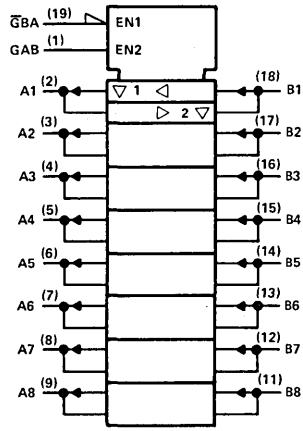
logic symbols

'HC620



'HC623



Pin numbers shown are for J and N packages.

3

maximum ratings, recommended operating conditions, and electrical characteristics

See Table III, page 2-5.

'HC620 switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 45 pF, R_L = 667Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, See Note 1				UNIT
						T_A = 25°C		SN54HC620	SN74HC620	
			MIN	TYP	MAX	MIN	TYP MAX	MIN MAX	MIN MAX	
t_{PLH}	A	B								ns
t_{PHL}										
t_{PLH}	B	A								ns
t_{PHL}										
t_{PZH}	$\overline{G}$BA	A								ns
t_{PZL}										
t_{PHZ}	$\overline{G}$BA	A								ns
t_{PLZ}										
t_{PZH}	GAB	B								ns
t_{PZL}										
t_{PHZ}	GAB	B								ns
t_{PLZ}										

C_{pd}	Power dissipation capacitance per transceiver	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

'HC623 switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 45 pF, R_L = 667Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, See Note 1				UNIT
						T_A = 25°C			SN54HC623	SN74HC623	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN MAX	MIN MAX	
t_{PLH}	A	B									ns
t_{PHL}											
t_{PLH}	B	A									ns
t_{PHL}											
t_{PZH}	$\overline{G}$BA	A									ns
t_{PZL}											
t_{PHZ}	$\overline{G}$BA	A									ns
t_{PLZ}											
t_{PZH}	GAB	B									ns
t_{PZL}											
t_{PHZ}	GAB	B									ns
t_{PLZ}											

C_{pd}	Power dissipation capacitance per transceiver	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

TEXAS INSTRUMENTS
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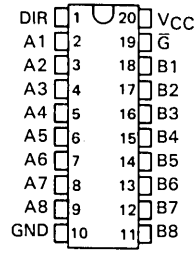
TYPES SN54HC640, SN54HC643, SN54HC645, SN74HC640, SN74HC643, SN74HC645 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

D2684, DECEMBER 1982

- **Bus Transceivers in High-Density 20-Pin DIPs and also Plastic and Ceramic Chip Carriers**
- **Choice of True or Inverting Logic**
- **High-Current 3-State Outputs Can Drive up to 15 LSTTL Loads**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	LOGIC
'HC640	Inverting
'HC643	True and Inverting
'HC645	True

SN54HC'. . . J PACKAGE
SN74HC'. . . J OR N PACKAGE
(TOP VIEW)

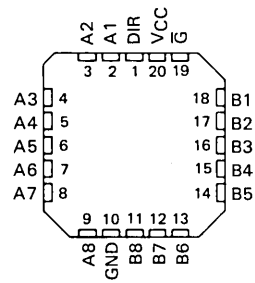


description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so the buses are effectively isolated.

The SN54HC640, SN54HC643 and SN54HC645 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC640, SN74HC643, and SN74HC645 are characterized for operation from −40°C to 85°C.

SN54HC'. . . FH OR FK PACKAGE
SN74HC'. . . FH OR FN PACKAGE
(TOP VIEW)



FUNCTION TABLE

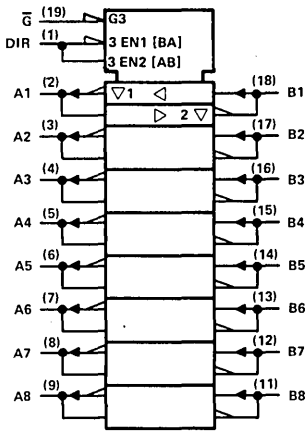
CONTROL INPUTS		OPERATION		
$\overline{G}$	DIR	'HC640	'HC645	'HC643
L	L	$\overline{B}$ data to A bus	B data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	A data to B bus	$\overline{A}$ data to B bus
H	X	Isolation	Isolation	Isolation

PRODUCT PREVIEW

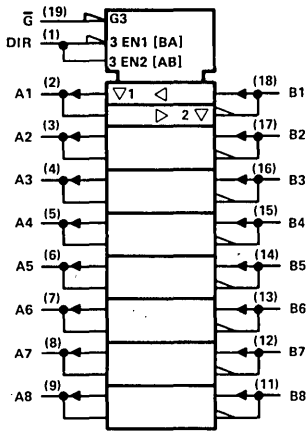
This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

logic symbols

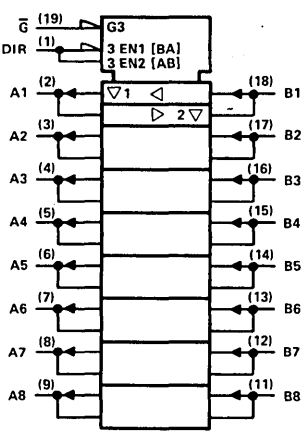
'HC640



'HC643



'HC645



Pin numbers shown are for J and N packages

maximum ratings, recommended operating conditions, and electrical characteristics

See Table III, page 2-5.

'HC640 switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 45 pF, R_L = 667Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, See Note 1				UNIT
						T_A = 25°C			SN54HC640	SN74HC640	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN MAX	MIN MAX	
t_{PLH}	A or B	B or A									ns
t_{PHL}											
t_{PZH}	$\overline{G}$	A or B									ns
t_{PZL}											
t_{PHZ}	$\overline{G}$	A or B									ns
t_{PLZ}											

C_{pd}	Power dissipation capacitance per transceiver	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

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'HC643 switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 45 pF, R_L = 667Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, See Note 1				UNIT
						T_A = 25°C		SN54HC643	SN74HC643	
			MIN	TYP	MAX	MIN	TYP MAX	MIN MAX	MIN MAX	
t_{PLH}	A	B								ns
t_{PHL}										
t_{PLH}	B	A								ns
t_{PHL}										
t_{PZH}	$\overline{G}$	A								ns
t_{PZL}										
t_{PHZ}	$\overline{G}$	A								ns
t_{PLZ}										
t_{PZH}	$\overline{G}$	B								ns
t_{PZL}										
t_{PHZ}	$\overline{G}$	B								ns
t_{PLZ}										

C_{pd}	Power dissipation capacitance per transceiver	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

3

'HC645 switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 45 pF, R_L = 667Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, See Note 1				UNIT
						T_A = 25°C		SN54HC645	SN74HC645	
			MIN	TYP	MAX	MIN	TYP MAX	MIN MAX	MIN MAX	
t_{PLH}	A or B	B or A								ns
t_{PHL}										
t_{PZH}	$\overline{G}$	A or B								ns
t_{PZL}										
t_{PHZ}	$\overline{G}$	A or B								ns
t_{PLZ}										

C_{pd}	Power dissipation capacitance per transceiver	No load, T_A = 25°C	pF typ

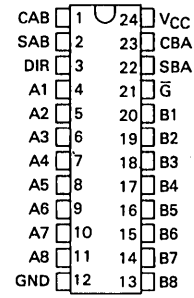
NOTE 1: For load circuit and voltage waveforms, see page 1-14.

TYPES SN54HC646, SN54HC648, SN74HC646, SN74HC648 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

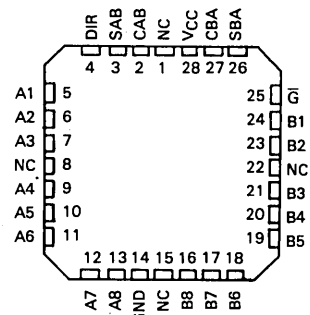
D2684, DECEMBER 1982

- **Independent Registers for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Choice of True or Inverting Data Paths**
- **High-Current 3-State Outputs Can Drive up to 15 LSTTL Loads**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC' . . . JT PACKAGE
SN74HC' . . . JT OR NT PACKAGE
(TOP VIEW)



SN54HC' . . . FH OR FK PACKAGE
SN74HC' . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

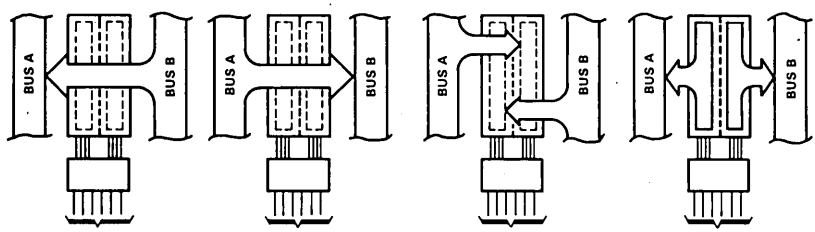
description

These devices consist of bus transceiver circuits with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock pin (CAB or CBA). The examples below demonstrate the four fundamental bus-management functions that can be performed with the 'HC646 or 'HC648.

Enable ($\overline{G}$) and direction (DIR) pins are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when enable $\overline{G}$ is active (low). In the isolation mode (enable $\overline{G}$ high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from −40°C to 85°C.



REAL-TIME TRANSFER BUS B TO BUS A

REAL-TIME TRANSFER BUS A TO BUS B

STORAGE FROM A, B, OR A AND B

TRANSFER STORED DATA TO A OR B

Pin numbers shown are for JT and NT packages.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

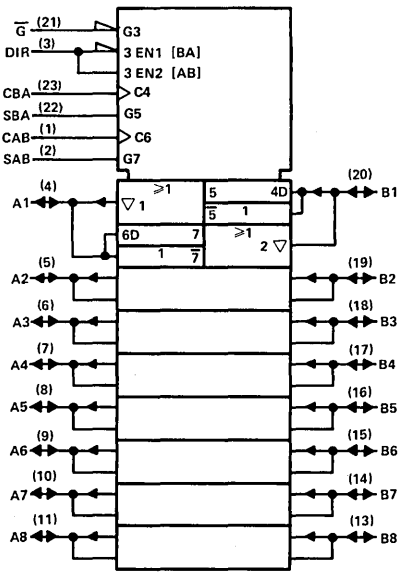
FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION	
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'HC646	'HC648
X	X	↑	X	X	X	Input	Not specified	Store A, B unspecified	Store A, B unspecified
X	X	X	↑	X	X	Not specified	Input	Store B, A unspecified	Store B, A unspecified
H	X	↑	↑	X	X	Input	Input	Store A and B Data	Store A and B Data
H	X	H or L	H or L	X	X			Isolation, hold storage	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus	Real-Time $\overline{B}$ Data to A Bus
L	L	X	X	X	H			Stored B Data to A Bus	Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus	Real-Time $\overline{A}$ Data to B Bus
L	H	X	X	H	X			Stored A Data to B Bus	Stored $\overline{A}$ Data to Bus

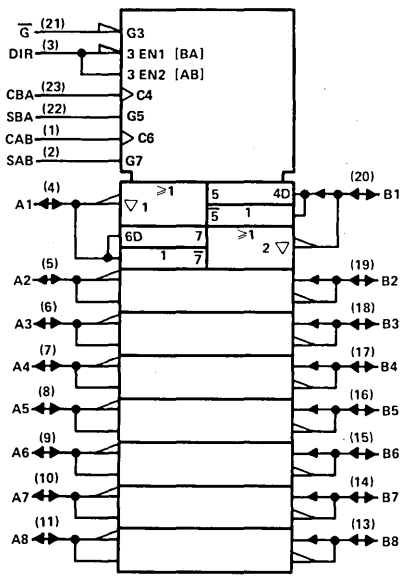
†The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

logic symbols

'HC646



'HC648



Pin numbers shown are for JT and NT packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table III, page 2-5.

timing requirements (supplement to recommended operating conditions)

			SN54HC'			SN74HC'			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}	Clock frequency								MHz
t_w	Clock pulse duration								ns
t_{su}	Setup time	A before CAB↑ or B before CBA↑							ns
t_h	Hold time	A after CAB↑ or B after CBA↑							ns

'HC646 switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 45 pF, R_L = 667Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, See Note 1					UNIT
						T_A = 25°C			SN54HC646	SN74HC646	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN MAX	MIN MAX	
f_{max}											MHz
t_{PLH}	CBA or CAB	A or B									ns
t_{PHL}											
t_{PLH}	A or B	B or A									ns
t_{PHL}											
t_{PLH}	SBA or SAB (with A or B high)†	A or B									ns
t_{PHL}											
t_{PLH}	SBA or SAB (with A or B low)†										
t_{PHL}											
t_{PZH}	$\overline{G}$	A or B									ns
t_{PZL}											
t_{PHZ}											
t_{PLZ}											
t_{PZH}	DIR	A or B									ns
t_{PZL}											
t_{PHZ}											
t_{PLZ}											

C_{pd}	Power dissipation capacitance per transceiver	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

†These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

TEXAS INSTRUMENTS
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'HC648 switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 45 pF, R_L = 667Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, See Note 1				UNIT
						T_A = 25°C		SN54HC648	SN74HC648	
			MIN	TYP	MAX	MIN	TYP MAX	MIN MAX	MIN MAX	
f_{max}										MHz
t_{PLH}	CBA or CAB	A or B								ns
t_{PHL}										
t_{PLH}	A or B	B or A								ns
t_{PHL}										
t_{PLH}	SBA or SAB (with A or B high)†	A or B								ns
t_{PHL}										
t_{PLH}	SBA or SAB (with A or B low)†									
t_{PHL}										
t_{PZH}	$\overline{G}$	A or B								ns
t_{PZL}										
t_{PHZ}										
t_{PLZ}										
t_{PZH}	DIR	A or B								ns
t_{PZL}										
t_{PHZ}										
t_{PLZ}										

C_{pd}	Power dissipation capacitance per transceiver	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

†These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

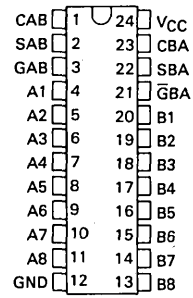
3

TYPES SN54HC651, SN54HC652, SN74HC651, SN74HC652
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

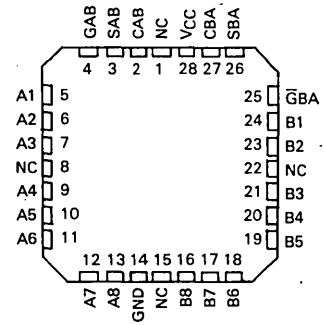
D2684, DECEMBER 1982

- Bus Transceivers/Registers
- Independent Registers and Enables for A and B Buses
- High-Current 3-State Outputs Can Drive up to 15 LSTTL Loads
- Multiplexed Real-Time and Stored Data
- Choice of True and Inverting Data Paths
- Included Among the Package Options Are Compact 24-Pin 300-mil-wide DIPs and Both 28-Pin Plastic and Ceramic Chip Carriers
- Dependable Texas Instruments Quality and Reliability

SN54HC651, SN54HC652 . . . JT PACKAGE
SN74HC651, SN54HC652 . . . JT OR NT PACKAGE
(TOP VIEW)



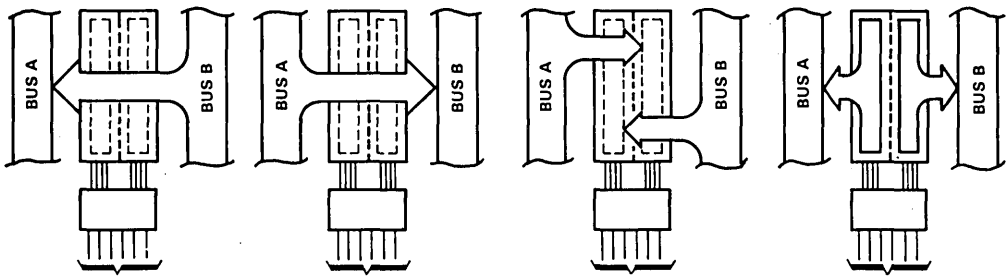
SN54HC651, SN74HC652 . . . FH OR FK PACKAGE
SN74HC651, SN74CH652 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enable GAB and GBA are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high selects stored data. The following examples demonstrate the four fundamental bus-management functions that can be performed with the 'HC651 and 'HC652.



REAL-TIME TRANSFER BUS B TO BUS A

REAL-TIME TRANSFER BUS A TO BUS B

STORAGE FROM A AND/OR B

TRANSFER STORED DATA TO A AND/OR B

Pin numbers shown are for JT and NT packages.

PRODUCT PREVIEW

TEXAS INSTRUMENTS
INCORPORATED
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Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and $\overline{\text{G}}$BA. In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

The SN54HC651 and SN54HC652 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC651 and SN74HC652 are characterized for operation from −40°C to 85°C.

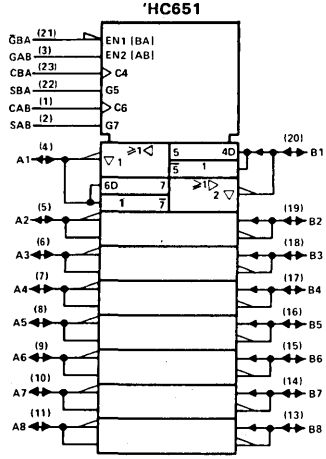
FUNCTION TABLE

INPUTS						DATA I/O*		OPERATION OR FUNCTION	
GAB	$\overline{\text{G}}$BA	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'HC651	'HC652
L	H	H or L	H or L	X	X	Input	Input	Isolation	Isolation
L	H	↑	↑	X	X			Store A and B Data	Store A and B Data
X	H	↑	H or L	X	X	Input	Not specified	Store A, Hold B	Store A, Hold B
H	H	↑	↑	X	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L	↑	X	X	Not specified	Input	Hold A, Store B	Hold A, Store B
L	L	↑	↑	X	X	Output	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time $\overline{\text{B}}$ Data to A Bus	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored $\overline{\text{B}}$ Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time $\overline{\text{A}}$ Data to B Bus	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored $\overline{\text{A}}$ Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{\text{A}}$ Data to B Bus and Stored $\overline{\text{B}}$ Data to A Bus	Stored A Data to B Bus and Stored B Data to A Bus

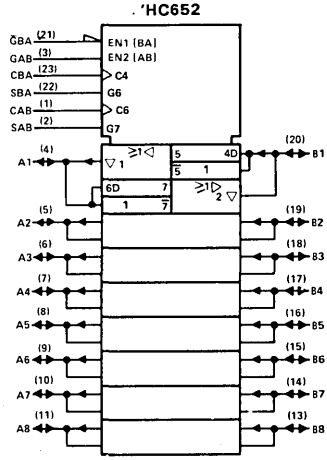
*The data output functions may be enabled or disabled by various signals at the GAB and $\overline{\text{G}}$BA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

logic symbols

'HC651



'HC652



Pin numbers shown are for JT and NT packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table III, page 2-5.

timing requirements (supplement to recommended operating conditions)

			SN54HC651 SN54HC652			SN74HC651 SN74HC652			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
t_w	Pulse duration	CBA or CAB high							ns
		CBA or CAB low							
t_{su}	Set up time before CAB or CBA↑	SBA or SAB							ns
		A or B							
t_w	Hold time after CAB or CBA↑	SBA or SAB							ns
		A or B							

'HC651 switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

3

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 45 pF, R_L = 667Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, See Note 1				UNIT
						T_A = 25°C		SN54HC651	SN74HC651	
			MIN	TYP	MAX	MIN	TYP MAX	MIN MAX	MIN MAX	
t_{PLH}	CBA or CAB	A or B								ns
t_{PHL}										
t_{PLH}	A or B	B or A								ns
t_{PHL}										
t_{PLH}	SBA or SAB↑ (with A or B high)	A or B								ns
t_{PHL}										
t_{PLH}	SBA or SAB↑ (with A or B low)	A or B								ns
t_{PHL}										
t_{PZH}	$\overline{G}$BA	A								ns
t_{PZL}										
t_{PHZ}	$\overline{G}$BA	A								ns
t_{PLZ}										
t_{PZH}	GAB	B								ns
t_{PZL}										
t_{PHZ}	GAB	B								ns
t_{PLZ}										

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.
†These parameters are measured with the internal output state of the storage register opposite to the that of the bus input.

TEXAS INSTRUMENTS
INCORPORATED
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'HC652 switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 45 pF, R_L = 667Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, See Note 1				UNIT
						T_A = 25°C		SN54HC652	SN74HC652	
			MIN	TYP	MAX	MIN	TYP MAX	MIN MAX	MIN MAX	
t_{PLH}	CBA or CAB	A or B								ns
t_{PHL}										
t_{PLH}	A or B	B or A								ns
t_{PHL}										
t_{PLH}	SBA or SAB† (with A or B high)	A or B								ns
t_{PHL}										
t_{PLH}	SBA or SAB† (with A or B low)	A or B								ns
t_{PHL}										
t_{PZH}	$\overline{G}$BA	A								ns
t_{PZL}										
t_{PHZ}	$\overline{G}$BA	A								ns
t_{PLZ}										
t_{PZH}	GAB	B								ns
t_{PZL}										
t_{PHZ}	GAB	B								ns
t_{PLZ}										

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.
†These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

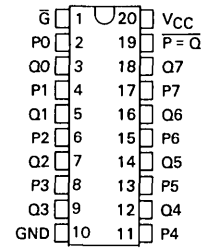
3

TYPES SN54HC688, SN74HC688
8-BIT IDENTITY COMPARATORS

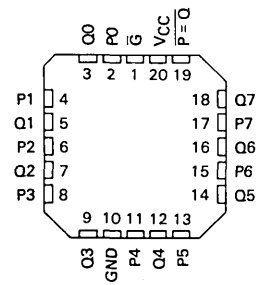
D2684, DECEMBER 1982

- *Compares Two Eight-Bit Words*
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC688 . . . J PACKAGE
SN74HC688 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC688 . . . FH OR FK PACKAGE
SN74HC688 . . . FH OR FN PACKAGE
(TOP VIEW)

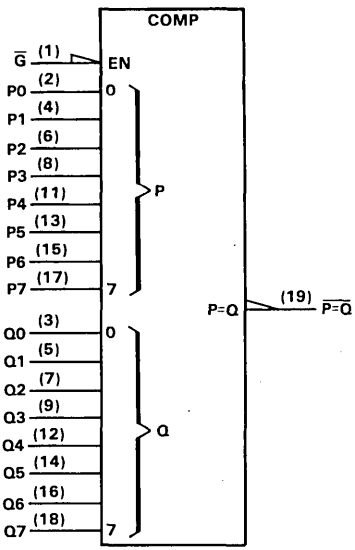


description

These identity comparators perform comparisons of two eight-bit binary or BCD words. An enable input ($\overline{G}$) may be used to force the output to the high level.

The SN54HC688 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC688 is characterized for operation from −40°C to 85°C.

logic symbol



Pin numbers shown are for J and N packages.

FUNCTION TABLE

INPUTS		OUTPUT
DATA P, Q	ENABLE $\overline{G}$	$\overline{P = Q}$
P = Q	L	L
P > Q	L	H
P < Q	L	H
X	H	H

maximum ratings, recommended operating conditions, and electrical characteristics

See Table IV, page 2-6.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF				UNIT
						T_A = 25°C		SN54HC688	SN74HC688	
			MIN	TYP	MAX	MIN	TYP MAX	MIN MAX	MIN MAX	
t_{PLH}	P	$\overline{P=Q}$								ns
t_{PHL}										
t_{PLH}	Q	$\overline{P=Q}$								ns
t_{PHL}										
t_{PLH}	$\overline{G}$	$\overline{P=Q}$								ns
t_{PHL}										

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

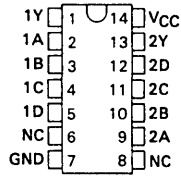
3

TYPES SN54HC4002, SN74HC4002
DUAL 4-INPUT POSITIVE-NOR GATES

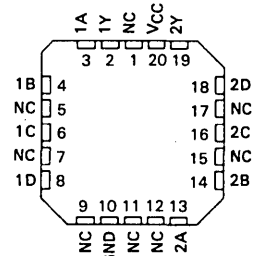
D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC4002 . . . J PACKAGE
SN74HC4002 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC4002 . . . FH OR FK PACKAGE
SN74HC4002 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

These devices contain two independent 4-input positive-NOR gates. They perform the boolean functions $Y = \overline{A + B + C + D}$ or $Y = \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D}$ in positive logic.

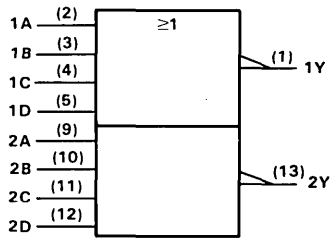
The SN54HC4002 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC4002 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
L	L	L	L	H
H	X	X	X	L
X	H	X	X	L
X	X	H	X	L
X	X	X	H	L

3

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table I, page 2-3.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF				UNIT
						T_A = 25°C		SN54HC'	SN74HC'	
			MIN	TYP	MAX	MIN	TYP MAX	MIN MAX	MIN MAX	
t_{PLH}	A thru D	Y								ns
t_{PHL}										

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

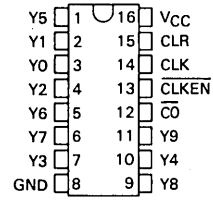
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TYPES SN54HC4017, SN74HC4017
DECADE COUNTERS/DIVIDERS

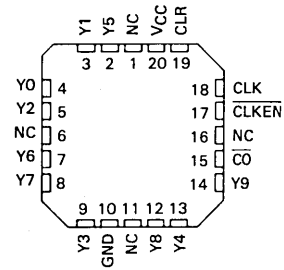
D2684, DECEMBER 1982

- Carry-Out Output for Cascading
- Divide-by-N Counting
- DC Clock Input Circuit Allows Slow Rise Times
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54HC4017 . . . J PACKAGE
SN74HC4017 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC4017 . . . FH OR FK PACKAGE
SN74HC4017 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

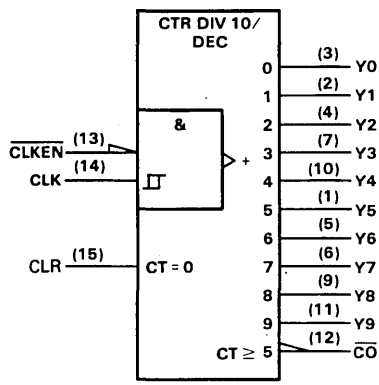
description

The 'HC4017 is a 5-stage divide-by-10 Johnson counter with ten decoded outputs and a carry-out bit. High-speed operation and spike-free outputs are obtained by use of the Johnson decade counter configuration.

The ten decoded outputs are normally low and go high only at their respective decimal time periods. A high signal on CLR asynchronously clears the decade counter and sets the carry output and Y0 high. With $\overline{\text{CLKEN}}$ low, the count is advanced on a low-to-high transition at CLK. Alternatively, if CLK is high, the count is advanced on a high-to-low transition at $\overline{\text{CLKEN}}$. Each decoded output remains high for one full clock cycle. The carry output is high while Y0, Y1, Y2, Y3, or Y4 is high, then is low while Y5, Y6, Y7, Y8, or Y9 is high.

The SN54HC4017 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74HC4017 is characterized for operation from -40°C to 85°C.

logic symbol

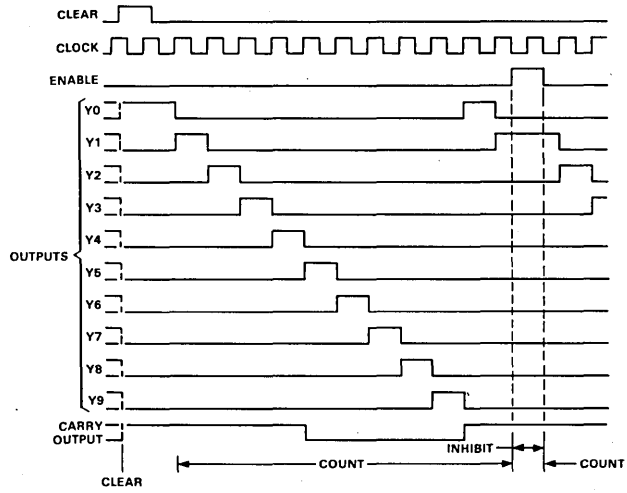


Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table IV, page 2-6.

typical clear, count, and inhibit sequences



timing requirements (supplement to recommended operating conditions)

			SN54HC4017			SN74HC4017			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	CLK high or low							ns
		CLR high							
t_{su}	Setup time, before CLK↑	$\overline{CLKEN}$ low							ns
		CLR inactive							

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF					UNIT
						T_A = 25°C			SN54HC'	SN74HC'	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN MAX	MIN MAX	
f_{max}											MHz
t_{PLH}	CLR	Any Y									ns
t_{PHL}											
t_{PLH}	CLK	$\overline{CO}$									ns
t_{PHL}											
t_{PLH}	CLK	Any Y									ns
t_{PHL}											
t_{PLH}	CLR	$\overline{CO}$									ns

C_{pd}	Power dissipation capacitance	No load; T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TYPES SN54HC4020, SN74HC4020
ASYNCHRONOUS 14-BIT BINARY COUNTERS

D2684, DECEMBER 1982

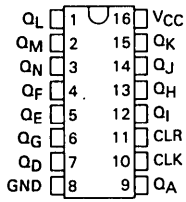
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

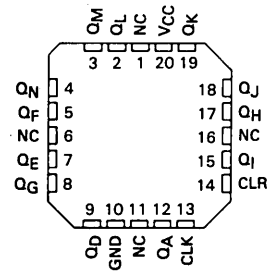
These devices are 14-stage binary ripple-carry counters that advance on the negative-going edge of the clock pulse. The counters are reset to zero (all outputs low) independently of the clock when CLR goes high.

The SN54HC4020 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC4020 is characterized for operation from −40°C to 85°C.

SN54HC4020 . . . J PACKAGE
SN74HC4020 . . . J OR N PACKAGE
(TOP VIEW)

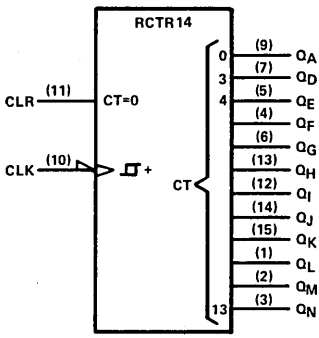


SN54HC4020 . . . FH OR FK PACKAGE
SN74HC4020 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table IV, page 2-6.

timing requirements (supplement to recommended operating conditions)

			SN54HC4020			SN74HC4020			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	CLK high or low							ns
		CLR high							
t_{su}	Setup time, CLR inactive before CLK↓								ns

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF				UNIT
						T_A = 25°C		SN54HC'	SN74HC'	
			MIN	TYP	MAX	MIN	TYP MAX	MIN MAX	MIN MAX	
f_{max}										MHz
t_{PLH}	CLK	Q_A								ns
t_{PHL}										
t_{PLH}	Qn	Qn + 1								ns
t_{PHL}										
t_{PHL}	CLR	Any								ns

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

3

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TYPES SN54HC4040, SN74HC4040
ASYNCHRONOUS 12-BIT BINARY COUNTERS

D2684, DECEMBER 1982

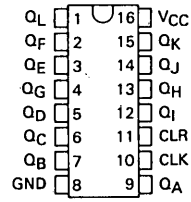
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

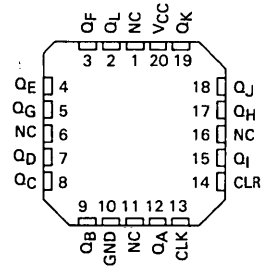
This device is an asynchronous 12-stage binary counter with the outputs of all stages available externally. A high level at CLR asynchronously clears the counter and resets all outputs low. The count is advanced on a high-to-low transition at CLK. Applications include time delay circuits, counter controls, and frequency-dividing circuits.

The SN54HC4040 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC4040 is characterized for operation from −40°C to 85°C.

SN54HC4040 . . . J PACKAGE
SN74HC4040 . . . J OR N PACKAGE
(TOP VIEW)

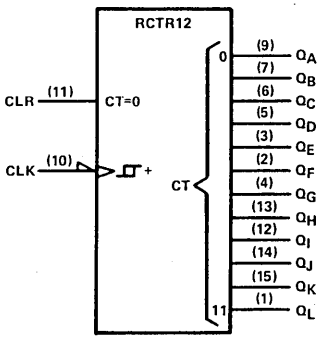


SN54HC4040 . . . FH OR FK PACKAGE
SN74HC4040 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table IV, page 2-6.

timing requirements (supplement to recommended operating conditions)

			SN54HC4040			SN74HC4040			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	CLK high or low							ns
		CLR high							
t_{su}	Setup time, CLR inactive before CLK↓								ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF				UNIT
						T_A = 25°C		SN54HC'	SN74HC'	
			MIN	TYP	MAX	MIN	TYP MAX	MIN MAX	MIN MAX	
f_{max}										MHz
t_{PLH}	CLK	Q_A								ns
t_{PHL}										
t_{PLH}	Qn	Qn + 1								ns
t_{PHL}										
t_{PHL}	CLR	Any								ns

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

3

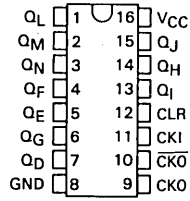
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TYPES SN54HC4060, SN74HC4060
ASYNCHRONOUS 14-STAGE BINARY COUNTERS AND OSCILLATORS

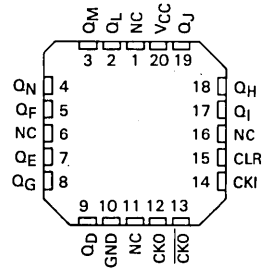
D2684, DECEMBER 1982

- **Allows Design of Either RC or Crystal Oscillator Circuits**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC4060 . . . J PACKAGE
SN74HC4060 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC4060 . . . FH OR FK PACKAGE
SN74HC4060 . . . FH OR FN PACKAGE
(TOP VIEW)



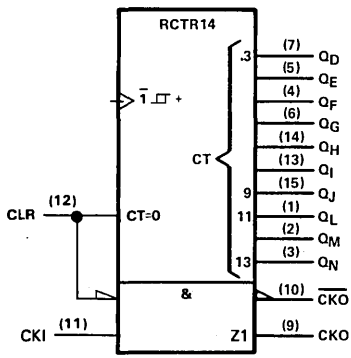
NC — No internal connection

description

The 'HC4060 consists of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC or crystal oscillator circuits. A negative transition on the clock input increments the counter. A high level at CLR disables the oscillator ($\overline{CKO}$ goes high and CKO goes low) and resets the counter to zero (all Q outputs low).

The SN54HC4060 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC4060 is characterized for operation from −40°C to 85°C.

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table IV, page 2-6.

timing requirements (supplement to recommended operating conditions)

			SN54HC4060			SN74HC4060			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
t_w	Pulse duration	CKI high or low							ns
		CLR high							
t_{su}	Setup time, CLR inactive before CKI↓								ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF					UNIT
						T_A = 25°C			SN54HC'	SN74HC'	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN MAX	MIN MAX	
f_{max}											MHz
t_{PLH}	CKI	Q_D									ns
t_{PHL}											
t_{PLH}	Qn	Qn+1									ns
t_{PHL}											
t_{PHL}	CLR	Any Q									ns

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

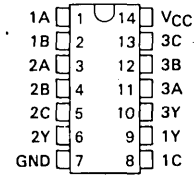
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TYPES SN54HC4075, SN74HC4075
TRIPLE 3-INPUT OR GATES

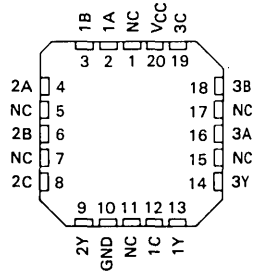
D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC4075 . . . J PACKAGE
SN74HC4075 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC4075 . . . FH OR FK PACKAGE
SN74HC4075 . . . FH OR FN PACKAGE
(TOP VIEW)



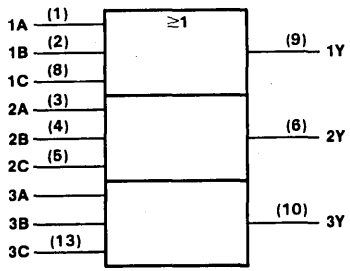
NC — No internal connection

description

These devices contain three independent 3-input OR gates and perform the boolean functions $Y = A + B + C$ or $Y = \overline{A \cdot B \cdot C}$ in positive logic.

The SN54HC4075 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC4075 is characterized for operation from −40°C to 85°C.

logic symbol



Pin numbers shown are for J and N packages.

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
H	X	X	H
X	H	X	H
X	X	H	H
L	L	L	L

maximum ratings, recommended operating conditions, and electrical characteristics

See Table I, page 2-3.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF						UNIT
						T_A = 25°C			SN54HC'		SN74HC'	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	MIN	MAX
t_{PLH}	A, B, or C	Y										ns
t_{PHL}												

C_{pd}	Power dissipation capacitance per gate	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

PRODUCT PREVIEW

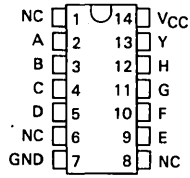
This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TYPES SN54HC4078, SN74HC4078 8-INPUT NOR GATE

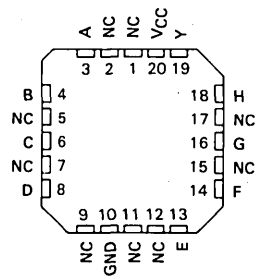
D2684, DECEMBER 1982

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC4078 . . . J PACKAGE
SN74HC4078 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC4078 . . . FH OR FK PACKAGE
SN74HC4078 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

These devices contain a single 8-input NOR gate and perform the following boolean functions in positive logic:

$$Y = \overline{A + B + C + D + E + F + G + H} \text{ or}$$

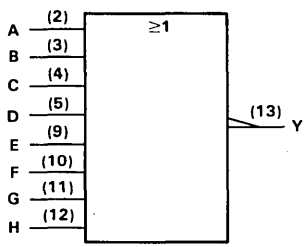
$$Y = \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D} \cdot \overline{E} \cdot \overline{F} \cdot \overline{G} \cdot \overline{H}$$

The SN54HC4078 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC4078 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS A THRU H	OUTPUT Y
All inputs L	H
One or more inputs H	L

logic symbol



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table I, page 2-3.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF				UNIT
						T_A = 25°C		SN54HC'	SN74HC'	
			MIN	TYP	MAX	MIN	TYP MAX	MIN MAX	MIN MAX	
t_{PLH}	A thru H	Y								ns
t_{PHL}										

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

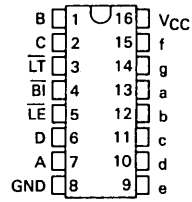
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TYPES SN54HC4511, SN74HC4511
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS
WITH LATCHED INPUTS

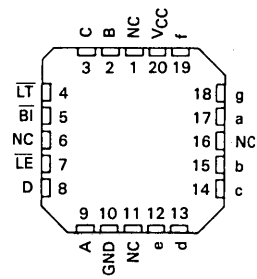
D2684, DECEMBER 1982

- Latch Storage of Code
- Blanking Input
- Lamp Test Provision
- Readout Blanking on All Illegal Input Combinations
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54HC4511 . . . J PACKAGE
SN74HC4511 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC4511 . . . FH OR FK PACKAGE
SN74HC4511 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

description

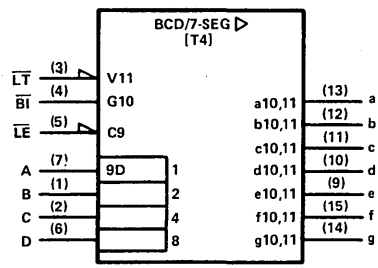
The 'HC4511 provides the functions of a 4-bit storage latch, a BCD-to-seven-segment decoder, and an output driver. Lamp test ($\overline{LT}$), blanking ($\overline{BI}$), and latch enable ($\overline{LE}$) inputs are used to test the display, to turn off or pulse-modulate the brightness of the display, and to store a BCD code, respectively.

The SN54HC4511 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC4511 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS							OUTPUTS							DISPLAY
$\overline{LE}$	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g	
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	H	L	L	H	H	9
L	H	H	H	L	H	L	L	L	L	L	L	L	L	Blank
L	H	H	H	L	H	H	L	L	L	L	L	L	L	Blank
L	H	H	H	H	L	L	L	L	L	L	L	L	L	Blank
L	H	H	H	H	L	H	L	L	L	L	L	L	L	Blank
L	H	H	H	H	H	L	L	L	L	L	L	L	L	Blank
L	H	H	H	H	H	H	L	L	L	L	L	L	L	Blank
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8
X	L	H	X	X	X	X	L	L	L	L	L	L	L	Blank
H	H	H	X	X	X	X	All outputs remain in state existing before $\overline{LE}$↑							

logic symbol

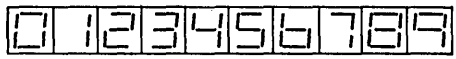


Pin numbers shown are for J and N packages.

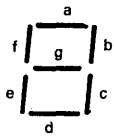
maximum ratings, recommended operating conditions, and electrical characteristics

See Table IV, page 2-6.

FONT TABLE T4 —
RESULTANT DISPLAYS USING 'HC4511



SEGMENT IDENTIFICATION



timing requirements (supplement to recommended operating conditions)

		SN54HC4511			SN74HC4511			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
t_w	Pulse duration, $\overline{LE}$ low							ns
t_{su}	Setup time, data before $\overline{LE}$↑							ns
t_h	Hold time, data after $\overline{LE}$↑							ns

3

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF						UNIT
						T_A = 25°C			SN54HC'		SN74HC'	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A thru D	a thru g											ns
t_{PHL}													
t_{PLH}	$\overline{BI}$	a thru g											ns
t_{PHL}													
t_{PLH}	$\overline{LT}$	a thru g											ns
t_{PHL}													
t_{PLH}	$\overline{LE}$	a thru g											ns
t_{PHL}													

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

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TYPES SN54HC4514, SN54HC4515, SN74HC4514, SN74HC4515

HIGH-SPEED CMOS LOGIC

4-LINE TO 16-LINE DECODERS/DEMULTIPLEXERS WITH ADDRESS LATCHES

D2684, DECEMBER 1982

- **Two Output Options:**
  'HC4514 Has Active-High Outputs
  'HC4515 Has Active-Low Outputs
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

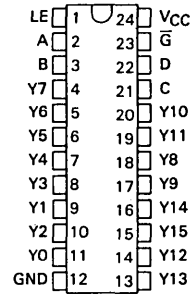
description

These devices present two output options of a 4-to-16 line decoder with latched inputs. The 'HC4514 presents a high level at the selected output. The 'HC4515 presents a low level at the selected output.

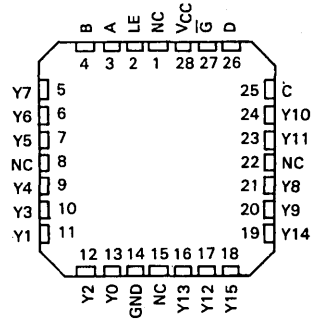
These devices consist of four storage latches with common latch enable (LE) and inhibit ($\overline{G}$) inputs. When a low signal is applied to the LE input, the input data is stored, decoded, and presented to the output. When LE is high, all sixteen 'HC4514 outputs are at a low logic level, or all 'HC4515 outputs are a high logic level.

The SN54HC4514 and the SN54HC4515 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74HC4514 and SN54HC4515 are characterized for operation from -40°C to 85°C.

SN54HC' . . . JT PACKAGE
SN74HC' . . . JT OR NT PACKAGE
(TOP VIEW)



SN54HC' . . . FH OR FN PACKAGE
SN74HC' . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

FUNCTION TABLE

INPUTS						OUTPUT SELECTED	OUTPUTS	
LE	$\overline{G}$	D	C	B	A		'HC4514	'HC4515
H	L	L	L	L	L	0		
H	L	L	L	L	H	1		
H	L	L	L	H	L	2		
H	L	L	L	H	H	3		
H	L	L	H	L	L	4		
H	L	L	H	L	H	5	Selected	Selected
H	L	L	H	H	L	6	Output = H	Output = L
H	L	L	H	H	H	7	All others = L	All others = H
H	L	H	L	L	L	8		
H	L	H	L	L	H	9		
H	L	H	L	H	L	10		
H	L	H	L	H	H	11		
H	L	H	H	L	L	12		
H	L	H	H	L	H	13		
H	L	H	H	H	L	14		
H	L	H	H	H	H	15		
X	H	X	X	X	X		All = L	All = H
L	L	X	X	X	X	All outputs remain in state existing before LE		

3

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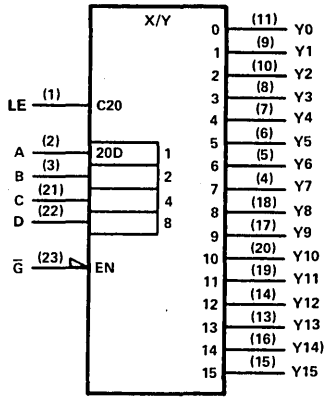
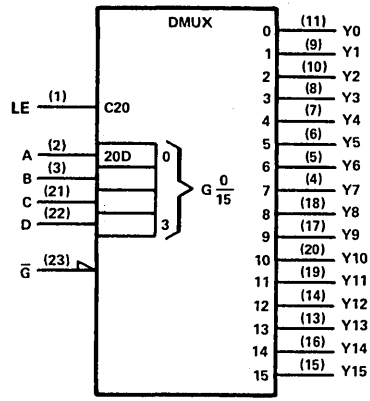
This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

'HC4514 logic symbols (alternatives)

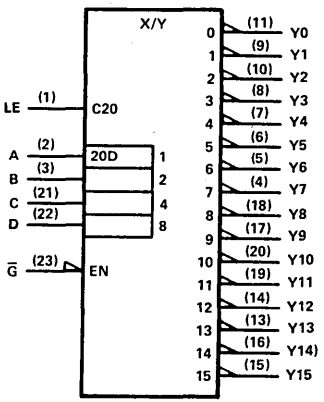


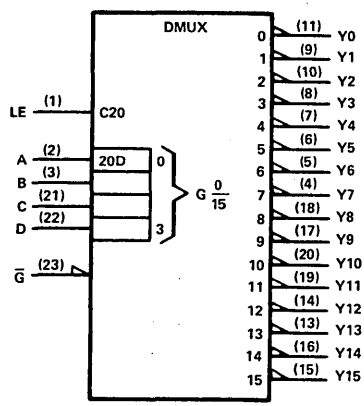


Pin numbers shown are for JT and NT packages.

3

'HC4515 logic symbols (alternatives)





Pin numbers shown are for JT and NT packages.

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maximum ratings, recommended operating conditions, and electrical characteristics

See Table IV, page 2-6.

timing requirements (supplement to recommended operating conditions)

		SN54HC'			SN74HC'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
t_w	Pulse duration, LE high							ns
t_{su}	Setup time before LE↓							ns
t_h	Hold time after LE↓							ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF						UNIT
						T_A = 25°C			SN54HC'		SN74HC'	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	MIN	MAX
t_{PLH}	A thru D	Any										ns
t_{PHL}												
t_{PLH}	LE	Any										ns
t_{PHL}												
t_{PLH}	$\overline{G}$	Any										ns
t_{PHL}												

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

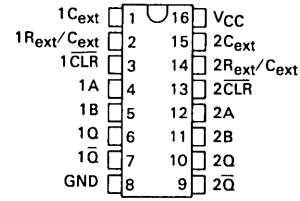
3

TYPES SN54HC4538, SN74HC4538
DUAL PRECISION RETRIGGERABLE/RESETTABLE MONOSTABLE MULTIVIBRATORS

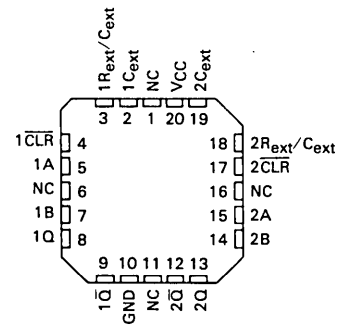
D2684, DECEMBER 1982

- Positive- and Negative-Edge Triggered Inputs with Hysteresis
- Complementary Outputs Available
- Independent Clear Inputs
- Wide Range of Output Pulse Durations
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54HC4538 . . . J PACKAGE
SN74HC4538 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC4538 . . . FH OR FK PACKAGE
SN74HC4538 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

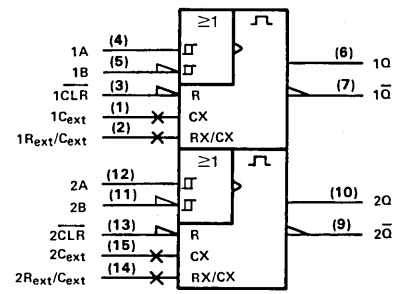
description

The 'HC4538 can be triggered by either the positive- or the negative edge of an input pulse. This device will produce an accurate output pulse over a wide range of pulse durations. The output pulse duration and accuracy are determined by the external timing components C_{ext} and R_{ext}. Trigger and clear propagation delays are independent of R_{ext} and C_{ext}.

A clear input is provided for immediate termination of the output pulse or to prevent output pulses when power is turned on.

The SN54HC4538 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC4538 is characterized for operation from −40°C to 85°C.

logic symbol



Pin numbers shown are for J and N packages.

FUNCTION TABLE

INPUTS			OUTPUTS	
CLEAR	A	B	Q	Q̄
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↓	⎍	⎎
H	↑	H	⎍	⎎

maximum ratings, recommended operating conditions, and electrical characteristics

See Table IV, page 2-6.

Note: The minimum recommended supply voltage for this device is 3 V.

PRODUCT PREVIEW

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timing requirements (supplement to recommended operating conditions)

		SN54HC4538			SN74HC4538			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
t_w	Pulse duration, A high or B low							MHz
R_{ext}	External timing resistance							kΩ
C_{ext}	External timing capacitance							μf

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF						UNIT
						T_A = 25°C			SN54HC'		SN74HC'	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}†	A	Q										ns
	B											
t_{PHL}†	A	Q										ns
	B											
t_{PHL}†	$\overline{CLR}$	Q										ns
t_{PLH}†		Q										
t_{wQ}(min)†	A or B	Q										ns
t_{wQ}‡	A or B	Q										μs

C_{pd}	Power dissipation capacitance per monostable	No load, T_A = 25°C	pF typ

†C_{ext} = 0, R_{ext} = 5kΩ
‡t_{wQ} = *duration of pulse at output Q.*
NOTE 1: For load circuit and voltage waveforms, see page 1-14.

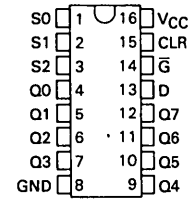
3

TYPES SN54HC4724, SN74HC4724
8-BIT ADDRESSABLE LATCHES

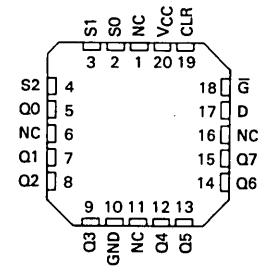
D2684, DECEMBER 1982

- 8-Bit Parallel-Out Storage Register Performs Serial-to-Parallel Conversion with Storage
- Asynchronous Parallel Clear
- Active-High Decoder
- Enable Input Simplifies Expansion
- Expandable for N-Bit Applications
- Four Distinct Functional Modes
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54HC4724 . . . J PACKAGE
SN74HC4724 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC4724 . . . FH OR FK PACKAGE
SN74HC4724 . . . FH OR FN PACKAGE
(TOP VIEW)



NC — No internal connection

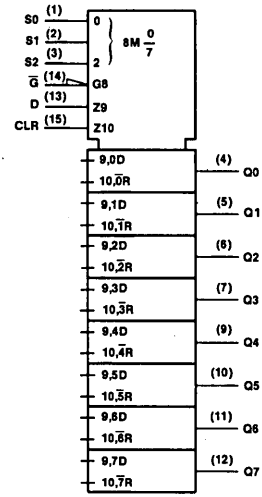
description

These 8-bit addressable latches are designed for general purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and active-high decoders or demultiplexers. They are multifunctional devices capable of storing single-line data in eight addressable latches, and being a 1-of-8 decoder or demultiplexer with active-high outputs.

Four distinct modes of operation are selectable by controlling the clear (CLR) and enable ($\overline{G}$) inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in terminal is written into the addressed latch. The addressed latch will follow the data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latches, enable $\overline{G}$ should be held high (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode, the addressed output will follow the level of the D input with all other outputs low. In the clear mode, all outputs are low and unaffected by the address and data inputs.

The SN54HC4724 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74HC4724 is characterized for operation from -40°C to 85°C.

logic symbol



Pin numbers shown are for J and N packages.

PRODUCT PREVIEW

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FUNCTION TABLE

INPUTS		OUTPUT OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
CLR	$\overline{G}$			
L	L	D	Q_{i0}	Addressable Latch
L	H	Q_{i0}	Q_{i0}	Memory
H	L	D	L	8-Line Demultiplexer
H	H	L	L	Clear

D = the level at the data input.
Q_{i0} = the level of Q_i (i = 0, 1, ...7, as appropriate) before the indicated steady-state input conditions were established.

LATCH SELECTION TABLE

SELECT INPUTS			LATCH ADDRESSED
S2	S1	S0	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

maximum ratings, recommended operating conditions, and electrical characteristics

See Table IV, page 2-6.

timing requirements (supplement to recommended operating conditions)

			SN54HC4724			SN74HC4724			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
t_w	Pulse duration	$\overline{G}$ low							ns
		CLR high							
t_{su}	Setup time before $\overline{G}$↑								ns
t_h	Hold time after $\overline{G}$↑								ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF					UNIT
						T_A = 25°C			SN54HC08	SN74HC08	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN MAX	MIN MAX	
t_{PHL}	CLR	Any									ns
t_{PLH}	Data	Any									ns
t_{PHL}											
t_{PLH}	Address	Any									ns
t_{PHL}											
t_{PLH}	$\overline{G}$	Any									ns
t_{PHL}											

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

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Explanation of Logic Symbols

4

TABLE OF CONTENTS

	Title	Page
1.	INTRODUCTION	4-3
2.	SYMBOL COMPOSITION	4-3
3.	QUALIFYING SYMBOLS	4-5
	3.1 General Qualifying Symbols	4-5
	3.2 Qualifying Symbols for Inputs and Outputs	4-5
	3.3 Symbols Inside the Outline	4-9
4.	DEPENDENCY NOTATION	4-10
	4.1 General Explanation	4-10
	4.2 G, AND	4-10
	4.3 Conventions for the Application of Dependency Notation in General	4-12
	4.4 V, OR	4-13
	4.5 N, Negate (Exclusive OR)	4-13
	4.6 Z, Interconnection	4-14
	4.7 C, Control	4-15
	4.8 S, Set and R, Reset	4-15
	4.9 EN, Enable	4-16
	4.10 M, Mode	4-17
	4.11 A, Address	4-19
5.	BISTABLE ELEMENTS	4-22
6.	CODERS	4-23
7.	USE OF A CODER TO PRODUCE AFFECTING INPUTS	4-24
8.	USE OF BINARY GROUPING TO PRODUCE AFFECTING INPUTS	4-25
9.	SEQUENCE OF INPUT LABELS	4-25
10.	SEQUENCE OF OUTPUT LABELS	4-26

4

LIST OF TABLES

Table	Title	Page
I.	General Qualifying Symbols	4-6
II.	Qualifying Symbols for Inputs and Outputs	4-7
III.	Symbols Inside the Outline	4-8
IV.	Summary of Dependency Notation	4-21

If you have questions on this Explanation of Logic Symbols, please contact:

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IEEE Standards may be purchased from:

Institute of Electrical and Electronics Engineers,
345 East 47th Street
New York, N.Y. 10017

International Electrotechnical Commission (IEC) publications may be purchased from:

American National Standards Institute, Inc.
1430 Broadway
New York, N.Y. 10018

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by F. A. Mann

1 INTRODUCTION

The International Electrotechnical Commission (IEC) has been developing a very powerful symbolic language that can show the relationship of each input of a digital logic circuit to each output without showing explicitly the internal logic. At the heart of the system is dependency notation, which will be explained in Section 4.

The system was introduced in the USA in a rudimentary form in IEEE/ANSI Standard Y32.14-1973. Lacking at that time a complete development of dependency notation, it offered little more than a substitution of rectangular shapes for the familiar distinctive shapes for representing the basic functions of AND, OR, negation, etc. This is no longer the case.

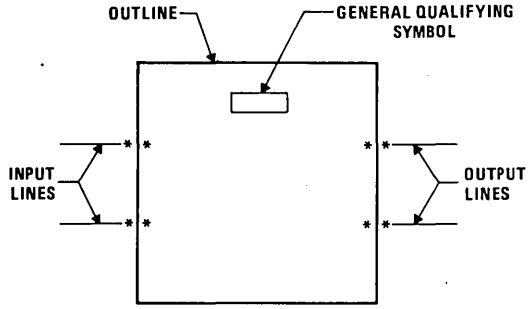
Internationally, Working Group 2 of IEC Technical Committee TC-3 is preparing a new document (Publication 617-12) that will consolidate the original work started in the mid 1960's and published in 1972 (Publication 117-15) and the amendments and supplements that have followed. Similarly for the USA, IEEE Committee SCC 11.9 is revising the publication IEEE Std 91/ANSI Y32.14. Texas Instruments is participating in the work of both organizations and this Data Book introduces new logic symbols in anticipation of the new standards. When changes are made as the standards develop, future editions will take those changes into account.

The following explanation of the new symbolic language is necessarily brief and greatly condensed from what the standards publications will finally contain. This is not intended to be sufficient for those people who will be developing symbols for new devices. It is primarily intended to make possible the understanding of the symbols used in this book; comparing the symbols with functional block diagrams and/or function tables will further help that understanding.

2 SYMBOL COMPOSITION

A symbol comprises an outline or a combination of outlines together with one or more qualifying symbols. The shape of the symbols is not significant. As shown in Figure 1, general qualifying symbols are used to tell exactly what logical operation is performed by the elements. Table I shows the general qualifying symbols used in this data book. Input lines are placed on the left and output lines are placed on the right. When an exception is made to that convention, the direction of signal flow is indicated by an arrow as shown in Figure 11.

All outputs of a single, unsubdivided element always have identical internal logic states determined by the function of the element except when otherwise indicated by an associated qualifying symbol or label inside the element.



*Possible positions for qualifying symbols relating to inputs and outputs

FIGURE 1 – SYMBOL COMPOSITION

The outlines of elements may be abutted or embedded in which case the following conventions apply. There is no logic connection between the elements when the line common to their outlines is in the direction of signal flow. There is at least one logic connection between the elements when the line common to their outlines is perpendicular to the direction of signal flow. The number of logic connections between elements will be clarified by the use of qualifying symbols and this is discussed further under that topic. If no indications are shown on either side of the common line, it is assumed there is only one connection.

When a circuit has one or more inputs that are common to more than one element of the circuit, the common-control block may be used. This is the only distinctively shaped outline used in the IEC system. Figure 2 shows that unless otherwise qualified by dependency notation, an input to the common-control block is an input to each of the elements below the common-control block.

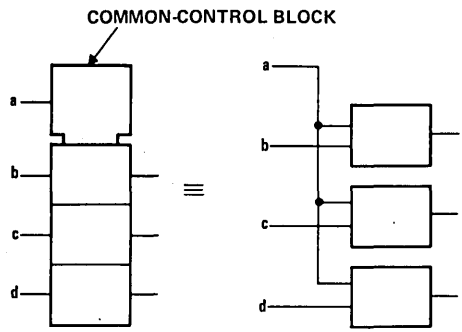


FIGURE 2 – ILLUSTRATION OF COMMON- CONTROL BLOCK

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A common output depending on all elements of the array can be shown as the output of a common-output element. Its distinctive visual feature is the double line at its top. In addition the common-output element may have other inputs as shown in Figure 3. The function of the common-output element must be shown by use of a general qualifying symbol.

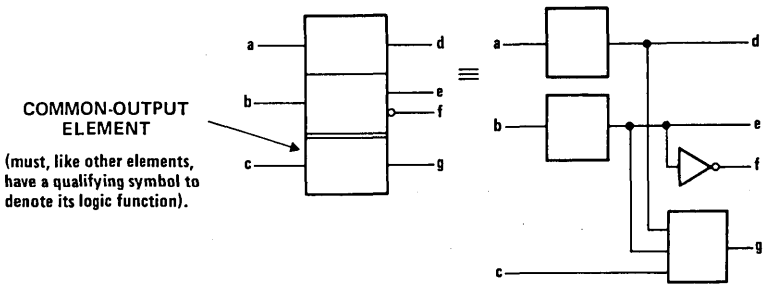

FIGURE 3 – ILLUSTRATION OF COMMON-OUTPUT ELEMENT

3 QUALIFYING SYMBOLS

3.1 General Qualifying Symbols

4

Table I shows the general qualifying symbols used in this data book. These characters are placed near the top center or the geometric center of a symbol or symbol element to define the basic function of the device represented by the symbol or of the element.

3.2 Qualifying Symbols for Inputs and Outputs

Qualifying symbols for inputs and outputs are shown in Table II and will be familiar to most users with the possible exception of the logic polarity and analog signal indicators. The older logic negation indicator means that the external 0 state produces the internal 1 state. The internal 1 state means the active state. Logic negation may be used in pure logic diagrams; in order to tie the external 1 and 0 logic states to the levels H (high) and L (low), a statement of whether positive logic (1 = H, 0 = L) or negative logic (1 = L, 0 = H) is being used is required or must be assumed. Logic polarity indicators eliminate the need for calling out the logic convention and are used in this data book in the symbology for actual devices. The presence of the triangular polarity indicator indicates that the L logic level will produce the internal 1 state (the active state) or that, in the case of an output, the internal 1 state will produce the external L level. Note how the active direction of transition for a dynamic input is indicated in positive logic, negative logic, and with polarity indication.

EXPLANATION OF LOGIC SYMBOLS

TABLE I – GENERAL QUALIFYING SYMBOLS

SYMBOL	DESCRIPTION	EXAMPLE
&	AND gate or function.	'HC00
>1	OR gate or function. The symbol was chosen to indicate that at least one active input is needed to activate the output.	'HC02
=1	Exclusive OR. One and only one input must be active to activate the output.	'HC86
=	Logic identity. All inputs must stand at same state.	'HC86
2k	An even number of inputs must be active.	'HC280
2k+1	An odd number of inputs must be active.	'HC86
1	The one input must be active.	'HC04
▷ or ◁	A buffer or element with more than usual output capability (symbol is oriented in the direction of signal flow).	'HC240
⊓	Schmitt trigger; element with hysteresis.	'HC132
X/Y	Coder, code converter (DEC/BCD, BIN/OUT, BIN/7-SEG, etc.).	'HC42
MUX	Multiplexer/data selector.	'HC151
DMUX or DX	Demultiplexer.	'HC138
Σ	Adder.	*
P–Q	Subtracter.	*
CPG	Look-ahead carry generator.	*
π	Multiplier.	*
COMP	Magnitude comparator.	'HC85
ALU	Arithmetic logic unit.	*
⌐⌐	Retriggerable monostable.	'HC123
1⌐⌐	Non-retriggerable monostable (one-shot).	'HC221
G	Astable element. Showing waveform is optional.	*
!G	Synchronously starting astable.	*
G!	Astable element that stops with a completed pulse.	*
SRGm	Shift register. m = number of bits.	'HC164
CTRm	Counter. m = number of bits; cycle length = 2^m.	'HC590
CTR DIVm	Counter with cycle length = m.	'HC160
RCTRm	Asynchronous (ripple-carry) counter; cycle length = 2^m.	'HC4020
ROM	Read-only memory.	*
RAM	Random-access read/write memory.	'HC189
FIFO	First-in, first-out memory.	*
I=0	Element powers up cleared to 0 state.	*
Φ	Highly complex function; "gray box" symbol with limited detail shown under special rules.	*

*Not all of the general qualifying symbols have been used in this book, but they are included here for the sake of completeness.

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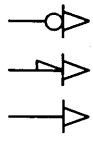
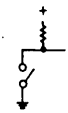
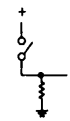
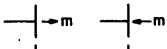
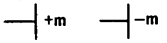
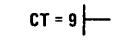
TABLE II – QUALIFYING SYMBOLS FOR INPUTS AND OUTPUTS

	Logic negation at input. External 0 produces internal 1.
	Logic negation at output. Internal 1 produces external 0.
	Active-low input. Equivalent to in positive logic.
	Active-low output. Equivalent to in positive logic.
	Active-low input in the case of right-to-left signal flow.
	Active-low output in the case of right-to-left signal flow.
	Signal flow from right to left. If not otherwise indicated, signal flow is from left to right.
	Bidirectional signal flow.
	Dynamic inputs active on indicated transition. POSITIVE LOGIC: 1→0, not used, 0→1. NEGATIVE LOGIC: 0→1, not used, 1→0. POLARITY INDICATION: not used, H→L, L→H.
	Nonlogic connection. A label inside the symbol will usually define the nature of this pin.
	Input for analog signals.
	Internal connection. 1 state on left produces 1 state on right.
	Negated internal connection. 1 state on left produces 0 state on right.
	Dynamic internal connection. Transition from 0 to 1 on left produces transitory 1 state on right.
	Internal input (virtual input). It always stands at its internal 1 state unless affected by an overriding dependency relationship.
	Internal output (virtual output). Its effect on an internal input to which it is connected is indicated by dependency notation.

The internal connections between logic elements abutted together in a symbol may be indicated by the symbols shown. Each logic connection may be shown by the presence of qualifying symbols at one or both sides of the common line and if confusion can arise about the numbers of connections, use can be made of one of the internal connection symbols.

The internal (virtual) input is an input originating somewhere else in the circuit and is not connected directly to a terminal. The internal (virtual) output is likewise not connected directly to a terminal.

TABLE III – SYMBOLS INSIDE THE OUTLINE

	Postponed output (of a pulse-triggered flip-flop). The output changes when input initiating change (e.g., a C input) returns to its initial external state or level. See § 5.
	Bi-threshold input (input with hysteresis)
	NPN open-collector or similar output that can supply a relatively low-impedance L level when not turned off. Requires external pull-up. Capable of positive-logic wired-AND connection. 
	Passive-pull-up output is similar to NPN open-collector output but is suplemented with a built-in passive pull-up.
	NPN open-emitter or similar output that can supply a relatively low-impedance H level when not turned off. Requires external pull-down. Capable of positive-logic wired-OR connection. 
	Passive-pull-down output is similar to NPN open-emitter output but is supplemented with a built-in passive pull-down.
	3-state output
	Output with more than usual output capability (symbol is oriented in the direction of signal flow).
	Enable input When at its internal 1-state, all outputs are enabled. When at its internal 0-state, open-collector and open-emitter outputs are off, three-state outputs are at normally defined internal logic states and at external high-impedance state, and all other outputs (e.g., totem-poles) are at the internal 0-state.
J, K, R, S, T	Usual meanings associated with flip-flops (e.g., R = reset, T = toggle)
	Data input to a storage element equivalent to: 
	Shift right (left) inputs, m = 1, 2, 3 etc. If m = 1, it is usually not shown.
	Counting up (down) inputs, m = 1, 2, 3 etc. If m = 1, it is usually not shown.
	Binary grouping. m is highest power of 2.
	The contents-setting input, when active, causes the content of a register to take on the indicated value.
	The content output is active if the content of the register is as indicated.
	Input line grouping . . . . indicates two or more terminals used to implement a single logic input. e.g., The paired expander inputs of SN7450. 
	Fixed-state output always stands at its internal 1 state. For example, see SN74185.

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The application of internal inputs and outputs requires an understanding of dependency notation, which is explained in Section 4.

In an array of elements, if the same general qualifying symbol and the same qualifying symbols associated with inputs and outputs would appear inside each of the elements of the array, these qualifying symbols are usually shown only in the first element. This is done to reduce clutter and to save time in recognition. Similarly, large identical elements that are subdivided into smaller elements may each be represented by an unsubdivided outline. The SN54HC242 symbol illustrates this principle.

3.3 Symbols Inside the Outline

Table III shows some symbols used inside the outline. Note particularly that open-collector, open-emitter, and three-state outputs have distinctive symbols. Also note that an EN input affects all of the outputs of the circuit and has no effect on inputs. When an enable input affects only certain outputs and/or affects one or more inputs, a form of dependency notation will indicate this (see 4.9). The effects of the EN input on the various types of outputs are shown.

It is particularly important to note that a D input is always the data input of a storage element. At its internal 1 state, the D input sets the storage element to its 1 state, and at its internal 0 state it resets the storage element to its 0 state.

The binary grouping symbol will be explained more fully in Section 8. Binary-weighted inputs are arranged in order and the binary weights of the least-significant and the most-significant lines are indicated by numbers. In this data book weights of input and output lines will be represented by powers of two usually only when the binary grouping symbol is used, otherwise, decimal numbers will be used. The grouped inputs generate an internal number on which a mathematical function can be performed or that can be an identifying number for dependency notation. See Figure 28. A frequent use is in addresses for memories.

Reversed in direction, the binary grouping symbol can be used with outputs. The concept is analogous to that for the inputs and the weighted outputs will indicate the internal number assumed to be developed within the circuit.

Other symbols are used inside the outlines in this data book in accordance with the IEC/IEEE standards but are not shown here. Generally these are associated with arithmetic operations and are self-explanatory.

When nonstandardized information is shown inside an outline, it is usually enclosed in square brackets [like these].

4 DEPENDENCY NOTATION

4.1 General Explanation

Dependency notation is the powerful tool that sets the IEC symbols apart from previous systems and makes compact, meaningful, symbols possible. It provides the means of denoting the relationship between inputs, outputs, or inputs and outputs without actually showing all the elements and interconnections involved. The information provided by dependency notation supplements that provided by the qualifying symbols for an element's function.

In the convention for the dependency notation, use will be made of the terms "affecting" and "affected". In cases where it is not evident which inputs must be considered as being the affecting or the affected ones (e.g., if they stand in an AND relationship), the choice may be made in any convenient way.

So far, ten types of dependency have been defined and all of these are used in this data book. They are listed below in the order in which they are presented and are summarized in Table IV following 4.11.

Section	Dependency Type or Other Subject
4.2	G, AND
4.3	General rules for dependency notation
4.4	V, OR
4.5	N, Negate, (Exclusive OR)
4.6	Z, Interconnection
4.7	C, Control
4.8	S, Set and R, Reset
4.9	EN, Enable
4.10	M, Mode
4.11	A, Address

4.2 G (AND) Dependency

A common relationship between two signals is to have them ANDed together. This has traditionally been shown by explicitly drawing an AND gate with the signals connected to the inputs of the gate. The 1972 IEC publication and the 1973 IEEE/ANSI standard showed several ways to show this AND relationship using dependency notation. While nine other forms of dependency have since been defined, the ways to invoke AND dependency are now reduced to one.

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In Figure 4 input **b** is ANDed with input **a** and the complement of **b** is ANDed with **c**. The letter G has been chosen to indicate AND relationships and is placed at input **b**, inside the symbol. A number considered appropriate by the symbol designer (1 has been used here) is placed after the letter G and also at each affected input. Note the bar over the 1 at input **c**.

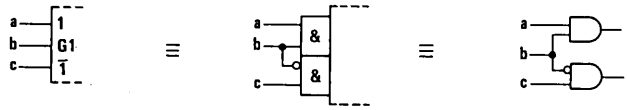

FIGURE 4 – G DEPENDENCY BETWEEN INPUTS

In Figure 5, output **b** affects input **a** with an AND relationship. The lower example shows that it is the internal logic state of **b**, unaffected by the negation sign, that is ANDed. Figure 6 shows input **a** to be ANDed with a dynamic input **b**.

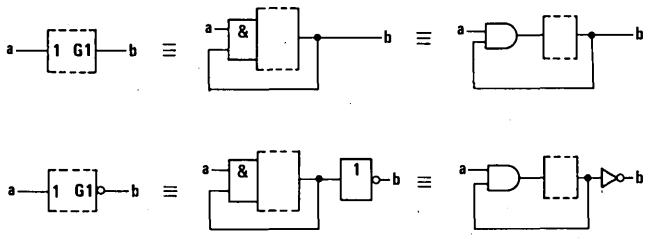

FIGURE 5 – G DEPENDENCY BETWEEN OUTPUTS AND INPUTS

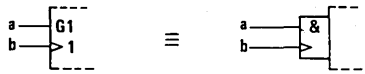

FIGURE 6 – G DEPENDENCY WITH A DYNAMIC INPUT

The rules for G dependency can be summarized thus:

When a G*m* input or output (*m* is a number) stands at its internal 1 state, all inputs and outputs affected by G*m* stand at their normally defined internal logic states. When the G*m* input or output stands at its 0 state, all inputs and outputs affected by G*m* stand at their internal 0 states.

4.3 Conventions for the Application of Dependency Notation in General

The rules for applying dependency relationships in general follow the same pattern as was illustrated for G dependency.

Application of dependency notation is accomplished by:

1) labeling the input (or output) *affecting* other inputs or outputs with the letter symbol indicating the relationship involved (e.g., G for AND) followed by an identifying number, appropriately chosen; and
2) labeling each input or output *affected* by that affecting input (or output) with that same number.

If it is the complement of the internal logic state of the affecting input or output that does the affecting, then a bar is placed over the identifying numbers at the affected inputs or outputs. See Figure 4.

If two affecting inputs or outputs have the same letter and same identifying number, they stand in an OR relationship to each other. See Figure 7.

4

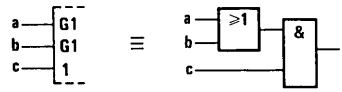

FIGURE 7 – OR'ED AFFECTING INPUTS

If the affected input or output requires a label to denote its function (e.g., "D"), this label will be *prefixed* by the identifying number of the affecting input. See Figure 12.

If an input or output is affected by more than one affecting input, the identifying numbers of each of the affecting inputs will appear in the label of the affected one, separated by commas. The normal reading order of these numbers is the same as the sequence of the affecting relationships. See Figure 12.

If the labels denoting the functions of affected inputs or outputs must be numbers, (e.g., outputs of a coder), the identifying numbers to be associated with both affecting inputs and affected inputs or outputs will be replaced by another character selected to avoid ambiguity, e.g., Greek letters. See Figure 8.

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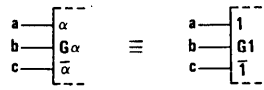


FIGURE 8 – SUBSTITUTION FOR NUMBERS

4.4 V (OR) Dependency

The symbol denoting OR dependency is the letter V. See Figure 9.

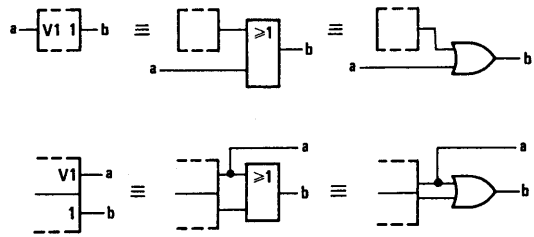
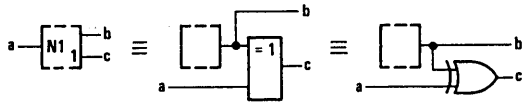


FIGURE 9 – V (OR) DEPENDENCY

When a V*m* input or output stands at its internal 1 state, all inputs and outputs affected by V*m* stand at their internal 1 states. When the V*m* input or output stands at its internal 0 state, all inputs and outputs affected by V*m* stand at their normally defined internal logic states.

4.5 N (Negate) (X-OR) Dependency

The symbol denoting negate dependency is the letter N. See Figure 10. Each input or output affected by an N*m* input or output stands in an exclusive-OR relationship with the N*m* input or output.



If a = 0, then c = b
If a = 1, then c = b

FIGURE 10 – N (NEGATE) (X-OR) DEPENDENCY

When an N*m* input or output stands at its internal 1 state, the internal logic state of each input and each output affected by N*m* is the complement of what it would otherwise be. When an N*m* input or output stands at its internal 0 state, all inputs and outputs affected by N*m* stand at their normally defined internal logic states.

4.6 Z (Interconnection) Dependency

The symbol denoting interconnection dependency is the letter Z.

Interconnection dependency is used to indicate the existence of internal logic connections between inputs, outputs, internal inputs, and/or internal outputs.

The internal logic state of an input or output affected by a Z*m* input or output will be the same as the internal logic state of the Z*m* input or output, unless modified by additional dependency notation. See Figure 11.

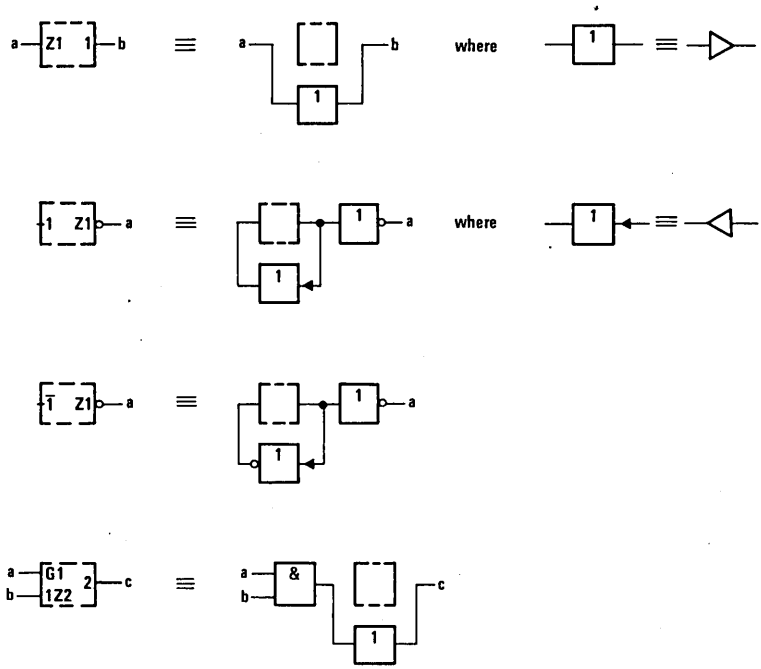


FIGURE 11 – Z (INTERCONNECTION) DEPENDENCY

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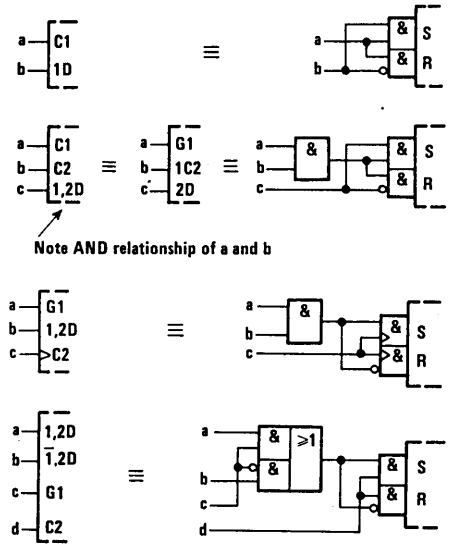
4.7 C (Control) Dependency

The symbol denoting control dependency is the letter C.

Control inputs are usually used to enable or disable the data (D, J, K, R, or S) inputs of storage elements. They may take on their internal 1 states (be active) either statically or dynamically. In the latter case the dynamic input symbol is used as shown in the third example of Figure 12.



Input c selects which of a or b is stored when d goes low.

FIGURE 12 – C (CONTROL) DEPENDENCY

When a C*m* input or output stands at its internal 1 state, the inputs affected by C*m* have their normally defined effect on the function of the element, i.e., these inputs are enabled. When a C*m* input or output stands at its internal 0 state, the inputs affected by C*m* are disabled and have no effect on the function of the element.

4.8 S (Set) and R (Reset) Dependencies

The symbol denoting set dependency is the letter S. The symbol denoting reset dependency is the letter R.

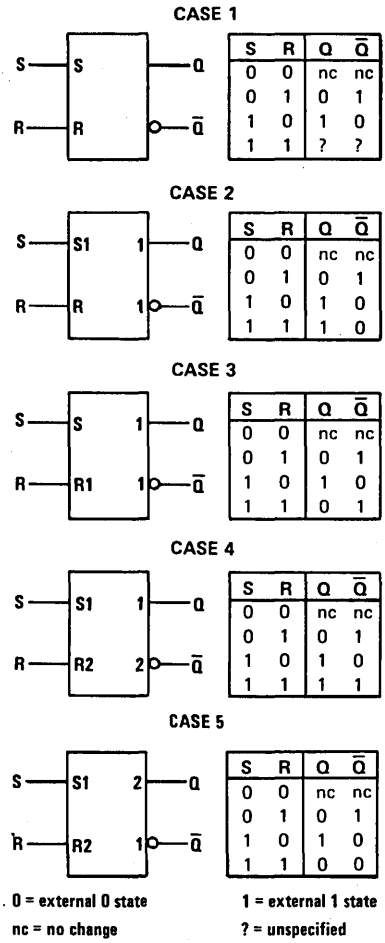
Set and reset dependencies are used if it is necessary to specify the effect of the combination R=S=1 on a bistable element. Case 1 in Figure 13 does not use S or R dependency.

When an S*m* input is at its internal 1 state, outputs affected by the Sm input will react, regardless of the state of an R input, as they normally would react to the combination S=1, R=0. See cases 2, 4, and 5 in Figure 13.

When an R*m* input is at its internal 1 state, outputs affected by the Rm input will react, regardless of the state of an S input, as they normally would react to the combination S=0, R=1. See cases 3, 4, and 5 in Figure 13.

When an S*m* or R*m* input is at its internal 0 state, it has no effect.

Note that the noncomplementary output patterns in cases 4 and 5 are only pseudo stable. The simultaneous return of the inputs to S=R=0 produces an unforeseeable stable and complementary output pattern.



S	R	Q	Q̄
0	0	nc	nc
0	1	0	1
1	0	1	0
1	1	?	?

S	R	Q	Q̄
0	0	nc	nc
0	1	0	1
1	0	1	0
1	1	1	0

S	R	Q	Q̄
0	0	nc	nc
0	1	0	1
1	0	1	0
1	1	0	1

S	R	Q	Q̄
0	0	nc	nc
0	1	0	1
1	0	1	0
1	1	1	1

S	R	Q	Q̄
0	0	nc	nc
0	1	0	1
1	0	1	0
1	1	0	0

FIGURE 13 – S (SET) AND R (RESET) DEPENDENCIES

4.9 EN (Enable) Dependency

The symbol denoting enable dependency is the combination of letters EN.

An EN*m* input has the same effect on outputs as an EN input, see 3.1, but it effects only those outputs labeled with the identifying number *m*. It also affects those inputs labeled with the identifying number *m*. By contrast, an EN input affects all outputs and no inputs. The effect of an EN*m* input on an affected input is identical to that of a C*m* input. See Figure 14.

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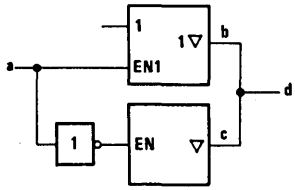
When an EN*m* input stands at its internal 1 state, the inputs affected by EN*m* have their normally defined effect on the function of the element and the outputs affected by this input stand at their normally defined internal logic states, i.e., these inputs and outputs are enabled.



If a = 0, b is disabled and d = c
If a = 1, c is disabled and d = b

FIGURE 14 – EN (ENABLE) DEPENDENCY

When an EN*m* input stands at its internal 0 state, the inputs affected by EN*m* are disabled and have no effect on the function of the element, and the outputs affected by EN*m* are also disabled. Open-collector outputs are turned off, three-state outputs stand at their normally defined internal logic states but externally exhibit high impedance, and all other outputs (e.g., totem-pole outputs) stand at their internal 0 states.

4.10 M (Mode) Dependency

The symbol denoting mode dependency is the letter M.

Mode dependency is used to indicate that the effects of particular inputs and outputs of an element depend on the mode in which the element is operating.

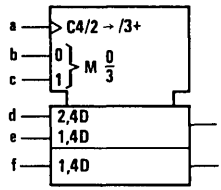
If an input or output has the same effect in different modes of operation, the identifying numbers of the relevant affecting M*m* inputs will appear in the label of that affected input or output between parentheses and separated by solidi. See Figure 19.

4.10.1 M Dependency Affecting Inputs

M dependency affects inputs the same as C dependency. When an M*m* input or M*m* output stands at its internal 1 state, the inputs affected by this M*m* input or M*m* output have their normally defined effect on the function of the element, i.e., the inputs are enabled.

When an M*m* input or M*m* output stands at its internal 0 state, the inputs affected by this M*m* input or M*m* output have no effect on the function of the element. When an affected input has several sets of labels separated by solidi (e.g., C4/2→/3+), any set in which the identifying number of the M*m* input or M*m* output appears has no effect and is to be ignored. This represents disabling of some of the functions of a multifunction input.

The circuit in Figure 15 has two inputs, **b** and **c**, that control which one of four modes (0, 1, 2, or 3) will exist at any time. Inputs **d**, **e**, and **f** are D inputs subject to dynamic control (clocking) by the **a** input. The numbers 1 and 2 are in the series chosen to indicate the modes so inputs **e** and **f** are only enabled in mode 1 (for parallel loading) and input **d** is only enabled in mode 2 (for serial loading). Note that input **a** has three functions. It is the clock for entering data. In mode 2, it causes right shifting of data, which means a shift away from the control block. In mode 3, it causes the contents of the register to be incremented by one count.



Note that all operations are synchronous.

In MODE 0 (b = 0, c = 0), the outputs remain at their existing states as none of the inputs has an effect.

In MODE 1 (b = 1, c = 0), parallel loading takes place thru inputs e and f.

In MODE 2 (b = 0, c = 1), shifting down and serial loading thru input d take place.

In MODE 3 (b = c = 1), counting up by increment of 1 per clock pulse takes place.

FIGURE 15 – M (MODE) DEPENDENCY AFFECTING INPUTS

4

4.10.2 M Dependency Affecting Outputs

When an M*m* input or M*m* output stands at its internal 1 state, the affected outputs stand at their normally defined internal logic states, i.e., the outputs are enabled.

When an M*m* input or M*m* output stands at its internal 0 state, at each affected output any set of labels containing the identifying number of that M*m* input or M*m* output has no effect and is to be ignored. When an output has several different sets of labels separated by solidi (e.g., 2,4/3,5), only those sets in which the identifying number of this M*m* input or M*m* output appears are to be ignored.

In Figure 16, mode 1 exists when the a input stands at its internal 1 state. The delayed output symbol is effective only in mode 1 (when input **a** = 1) in which case the device functions as a pulse-triggered flip-flop. See Section 5. When input **a** = 0, the device is not in mode 1 so the delayed output symbol has no effect and the device functions as a transparent latch.

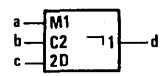


FIGURE 16 – TYPE OF FLIP-FLOP DETERMINED BY MODE

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In Figure 17, if input **a** stands at its internal 1 state establishing mode 1, output **b** will stand at its internal 1 state only when the content of the register equals 9. Since output **b** is located in the common-control block with no defined function outside of mode 1, the state of this output outside of mode 1 is not defined by the symbol.

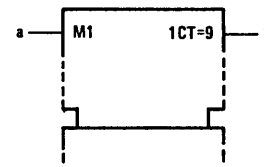

FIGURE 17 – DISABLING AN OUTPUT OF THE COMMON-CONTROL BLOCK

In Figure 18, if input **a** stands at its internal 1 state establishing mode 1, output **b** will stand at its internal 1 state only when the content of the register equals 15. If input **a** stands at its internal 0 state, output **b** will stand at its internal 1 state only when the content of the register equals 0.

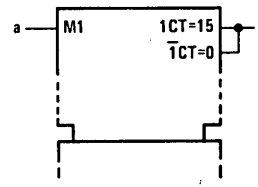

FIGURE 18 – DETERMINING AN OUTPUT'S FUNCTION

In Figure 19 inputs **a** and **b** are binary weighted to generate the numbers 0, 1, 2, or 3. This determines which one of the four modes exists.

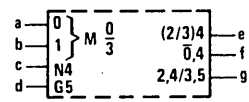

FIGURE 19 – DEPENDENT RELATIONSHIPS AFFECTED BY MODE

At output **e** the label set causing negation (if **c** = 1) is effective only in modes 2 and 3. In modes 0 and 1 this output stands at its normally defined state as if it had no labels. At output **f** the label set has effect when the mode is not 0 so output **e** is negated (if **c** = 1) in modes 1, 2, and 3. In mode 0 the label set has no effect so the output stands at its normally defined state. In this example 0,4 is equivalent to (1/2/3)4. At output **g** there are two label sets. The first set, causing negation (if **c** = 1), is effective only in mode 2. The second set, subjecting **g** to AND dependency on **d**, has effect only in mode 3.

Note that in mode 0 none of the dependency relationships has any effect on the outputs, so **e**, **f**, and **g** will all stand at the same state.

4.11 A (Address) Dependency

The symbol denoting address dependency is the letter A.

Address dependency provides a clear representation of those elements, particularly memories, that use address control inputs to select specified sections of a multidimensional array. Such a section of a memory array is usually called a word. The purpose of address dependency is to allow a symbolic presentation of the entire array. An input of the array shown at a particular element of this general section is common to the corresponding elements of all selected sections of the array. An output of the array shown at a particular element of this general section is the result of the OR function of the outputs of the corresponding elements of selected sections. If the label of an output of the array shown at a particular element of this general section indicates that this output is an open-circuit output or a three-state output, then this indication refers to the output of the array and not to those of the sections of the array.

Inputs that are not affected by any affecting address input have their normally defined effect on all sections of the array, whereas inputs affected by an address input have their normally defined effect only on the section selected by that address input.

An affecting address input is labelled with the letter A followed by an identifying number that corresponds with the address of the particular section of the array selected by this input. Within the general section presented by the symbol, inputs and outputs affected by an A*m* input are labelled with the letter A, which stands for the identifying numbers, i.e., the addresses, of the particular sections.

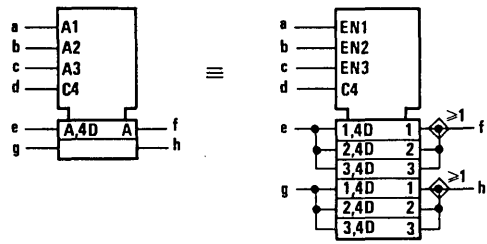

FIGURE 20 – A (ADDRESS) DEPENDENCY

Figure 20 shows a 3-word by 2-bit memory having a separate address line for each word and uses EN dependency to explain the operation. To select word 1, input a is taken to its 1 state, which establishes mode 1. Data can now be clocked into the inputs marked "1,4D". Unless words 2 and 3 are also selected, data cannot be clocked in at the inputs marked "2,4D" and "3,4D". The outputs will be the OR functions of the selected outputs, i.e., only those enabled by the active EN functions.

The identifying numbers of affecting address inputs correspond with the addresses of the sections selected by these inputs. They need not necessarily differ from those of other affecting dependency-inputs (e.g., G, V, N, . . .), because in the general section presented by the symbol they are replaced by the letter A.

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If there are several sets of affecting *Am* inputs for the purpose of independent and possibly simultaneous access to sections of the array, then the letter A is modified to 1A, 2A, . . . Because they have access to the same sections of the array, these sets of A inputs may have the same identifying numbers.

Figure 21 is another illustration of the concept.

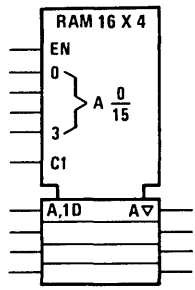

FIGURE 21

FIGURE 21 – ARRAY OF 16 SECTIONS OF FOUR TRANSPARENT LATCHES WITH 3-STATE OUTPUTS COMPRISING A 16-WORD X 4-BIT RANDOM-ACCESS MEMORY

4

TABLE IV – SUMMARY OF DEPENDENCY NOTATION

TYPE OF DEPENDENCY	LETTER SYMBOL*	AFFECTING INPUT AT ITS 1-STATE	AFFECTING INPUT AT ITS 0-STATE
Address	A	Permits action (address selected)	Prevents action (address not selected)
Control	C	Permits action	Prevents action
Enable	EN	Permits action	Prevents action of inputs. ◇outputs off. ▽outputs at external high impedance, no change in internal logic state. Other outputs at internal 0 state.
AND	G	Permits action	Imposes 0 state
Mode	M	Permits action (mode selected)	Prevents action (mode not selected)
Negate (X-OR)	N	Complements state	No effect
RESET	R	Affected output reacts as it would to S = 0, R = 1	No effect
SET	S	Affected output reacts as it would to S = 1, R = 0	No effect
OR	V	Imposes 1 state	Permits action
Interconnection	Z	Imposes 1 state	Imposes 0 state

*These letter symbols appear at the AFFECTING input (or output) and are followed by a number. Each input (or output) AFFECTED by that input is labeled with that same number. When the labels EN, R, and S appear at inputs without the following numbers, the descriptions above do not apply. The action of these inputs is described under "Symbols Inside The Outline", see 3.1.

BISTABLE ELEMENTS

The dynamic input symbol, the postponed output symbol, and dependency notation provide the tools to differentiate four main types of bistable elements and make synchronous and asynchronous inputs easily recognizable. See Figure 22. The first column shows the essential distinguishing features; the other columns show examples.

Transparent latches have a level-operated control input. The D input is active as long as the C input is at its internal 1 state. The outputs respond immediately. Edge-triggered elements accept data from D, J, K, R, or S inputs on the active transition of C. Pulse-triggered elements require the setup of data before the start of the control pulse; the C input is considered static since the data must be maintained as long as C is at its 1 state. The output is postponed until C returns to its 0 state. The data-lock-out element is similar to the pulse-triggered version except that the C input is considered dynamic in that shortly after C goes through its active transition, the data inputs are disabled and data does not have to be held. However, the output is still postponed until the C input returns to its initial external level.

Notice that synchronous inputs can be readily recognized by their dependency labels (1D, 1J, 1K, 1S, 1R) compared to the asynchronous inputs (S, R), which are not dependent on the C inputs.

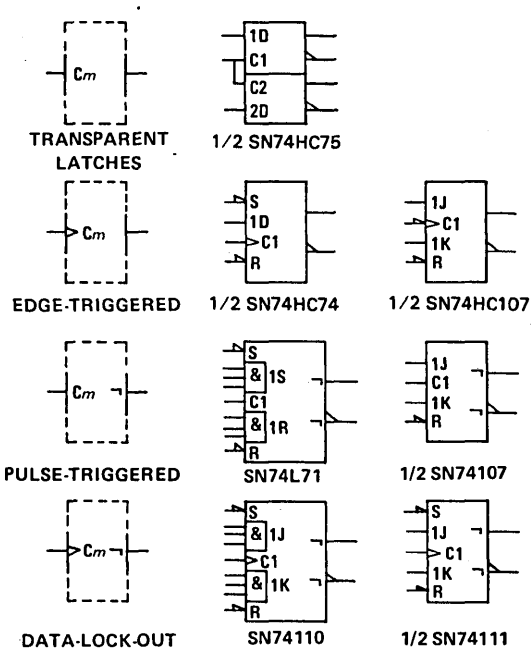

FIGURE 22 – FOUR TYPES OF BISTABLE CIRCUITS

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6 CODERS

The general symbol for a coder or code converter is shown in Figure 23. X and Y may be replaced by appropriate indications of the code used to represent the information at the inputs and at the outputs, respectively.

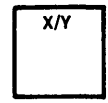


FIGURE 23 – CODER GENERAL SYMBOL

Indication of code conversion is based on the following rule:

> Depending on the input code, the internal logic states of the inputs determine an internal value. This value is reproduced by the internal logic states of the outputs, depending on the output code.

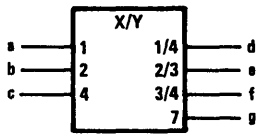
The indication of the relationships between the internal logic states of the inputs and the internal value is accomplished by:

1) labelling the inputs with numbers. In this case the internal value equals the sum of the weights associated with those inputs that stand at their internal 1-state, or by
2) replacing X by an appropriate indication of the input code and labelling the inputs with characters that refer to this code.

The relationships between the internal value and the internal logic states of the outputs are indicated by:

1) labelling each output with a list of numbers representing those internal values that lead to the internal 1-state of that output. These numbers shall be separated by solidi as in Figure 24. This labelling may also be applied when Y is replaced by a letter denoting a type of dependency (see Section 7). If a continuous range of internal values produces the internal 1 state of an output, this can be indicated by two numbers that are inclusively the beginning and the end of the range, with these two numbers separated by three dots, e.g., 4 . . . 9 = 4/5/6/7/8/9, or by
2) replacing Y by an appropriate indication of the output code and labelling the outputs with characters that refer to this code as in Figure 25.

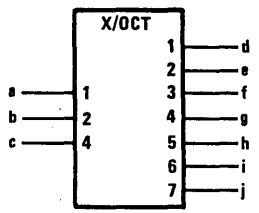
Alternatively, the general symbol may be used together with an appropriate reference to a table in which the relationship between the inputs and outputs is indicated. This is a recommended way to symbolize a PROM after it has been programmed.



FUNCTION TABLE

INPUTS			OUTPUTS			
c	b	a	g	f	e	d
0	0	0	0	0	0	0
0	0	1	0	0	0	1
0	1	0	0	0	1	0
0	1	1	0	1	1	0
1	0	0	0	1	0	1
1	0	1	0	0	0	0
1	1	0	0	0	0	0
1	1	1	1	0	0	0

FIGURE 24 – AN X/Y CODE CONVERTER



FUNCTION TABLE

INPUTS			OUTPUTS						
c	b	a	j	i	h	g	f	e	d
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	1	0
0	1	1	0	0	0	0	1	0	0
1	0	0	0	0	0	1	0	0	0
1	0	1	0	0	1	0	0	0	0
1	1	0	0	1	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0

FIGURE 25 – AN X/OCTAL CODE CONVERTER

7 USE OF A CODER TO PRODUCE AFFECTING INPUTS

It often occurs that a set of affecting inputs for dependency notation is produced by decoding the signals on certain inputs to an element. In such a case use can be made of the symbol for a coder as an embedded symbol. See Figure 26.

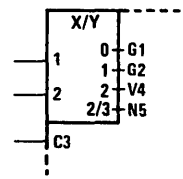


FIGURE 26 – PRODUCING VARIOUS TYPES OF DEPENDENCIES

If all affecting inputs produced by a coder are of the same type and their identifying numbers correspond with the numbers shown at the outputs of the coder, Y (in the qualifying symbol X/Y) may be replaced by the letter denoting the type of dependency. The indications of the affecting inputs should then be omitted. See Figure 27.

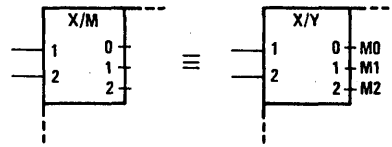


FIGURE 27 – PRODUCING ONE TYPE OF DEPENDENCY

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8 USE OF BINARY GROUPING TO PRODUCE AFFECTING INPUTS

If all affecting inputs produced by a coder are of the same type and have consecutive identifying numbers not necessarily corresponding with the numbers that would have been shown at the outputs of the coder, use can be made of the binary grouping symbol (see 3.1). k external lines effectively generate 2^k internal inputs. The bracket is followed by the letter denoting the type of dependency followed by $\frac{m1}{m2}$. The m1 is to be replaced by the smallest identifying number and the m2 by the largest one, as shown in Figure 28.

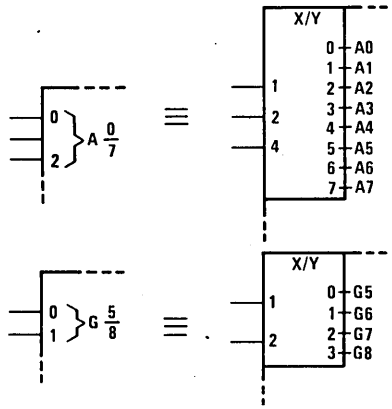

FIGURE 28 – USE OF THE BINARY GROUPING SYMBOL

9 SEQUENCE OF INPUT LABELS

If an input having a single functional effect is affected by other inputs, the qualifying symbol (if there is any) for that functional effect is preceded by the labels corresponding to the affecting inputs. The left-to-right order of these preceding labels is the order in which the effects or modifications must be applied. The affected input has no functional effect on the element if the logic state of any one of the affecting inputs, considered separately, would cause the affected input to have no effect, regardless of the logic states of other affecting inputs.

If an input has several different functional effects or has several different sets of affecting inputs, depending on the mode of action, the input may be shown as often as required. However, there are cases in which this method of presentation is not advantageous. In those cases the input may be shown once with the different sets of labels separated by solidi. See Figure 29. No meaning is attached to the order of these sets of labels. If one of the functional effects of an input is that of an unlabelled input of the element, a solidus will precede the first set of labels shown.

If all inputs of a combinational element are disabled (caused to have no effect on the function of the element), the internal logic states of the outputs of the element are not specified by the symbol. If all inputs of a sequential element are disabled, the content of this element is not changed and the outputs remain at their existing internal logic states.

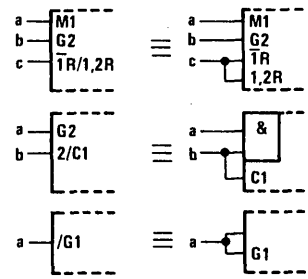

FIGURE 29 – INPUT LABELS

Labels may be factored using algebraic techniques.

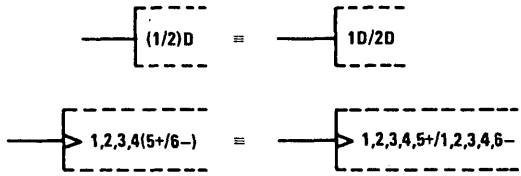

FIGURE 30 – FACTORING INPUT LABELS

10 SEQUENCE OF OUTPUT LABELS

If an output has a number of different labels, regardless of whether they are identifying numbers of affecting inputs or outputs or not, these labels are shown in the following order:

1) if the postponed output symbol has to be shown, this comes first, if necessary preceded by the indications of the inputs to which it must be applied;

2) followed by the labels indicating modifications of the internal logic state of the output, such that the left-to-right order of these labels corresponds with the order in which their effects must be applied;

3) followed by the label indicating the effect of the output on inputs and other outputs of the element.

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Symbols for open-circuit or three-state outputs, where applicable, are placed just inside the outside boundary of the symbol adjacent to the output line. See Figure 31.

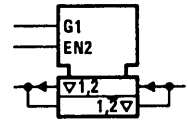

FIGURE 31 – PLACEMENT OF 3-STATE SYMBOLS

If an output needs several different sets of labels that represent alternative functions (e.g., depending on the mode of action), these sets may be shown on different output lines that must be connected outside the outline. However, there are cases in which this method of presentation is not advantageous. In those cases the output may be shown once with the different sets of labels separated by solidi. See Figure 32.

Two adjacent identifying numbers of affecting inputs in a set of labels that are not already separated by a nonnumeric character should be separated by a comma.

If a set of labels of an output not containing a solidus contains the identifying number of an affecting M*m* input standing at its internal 0 state, this set of labels has no effect on that output.

Labels may be factored using algebraic techniques.

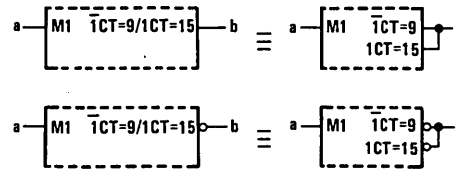

FIGURE 32 – OUTPUT LABELS

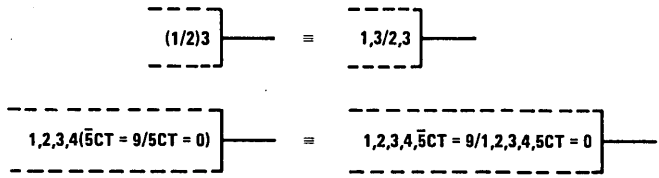

FIGURE 33 – FACTORING OUTPUT LABELS

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TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

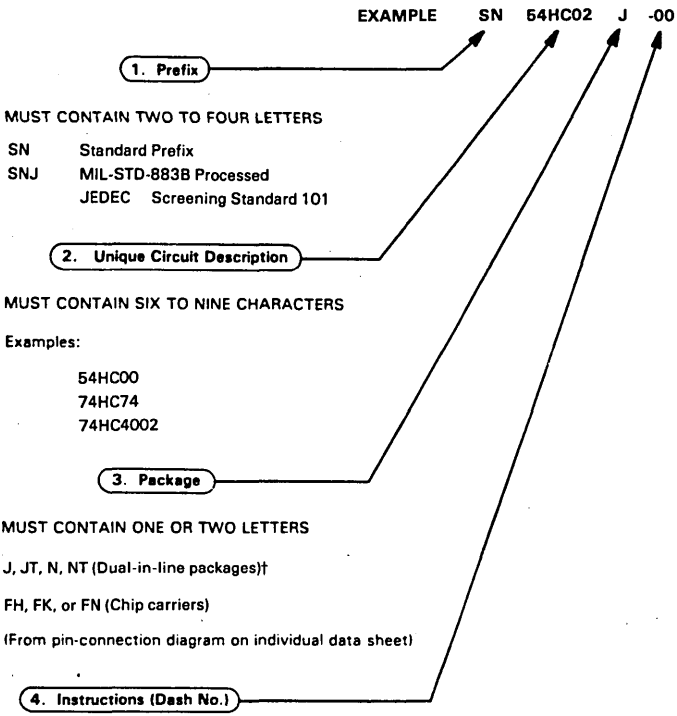
Ordering Instructions and Mechanical Data

5

ORDERING INSTRUCTIONS

Electrical characteristics presented in this data book, unless otherwise noted, apply for circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this catalog should include a four-part type number as explained in the following example.



† These circuits in dual-in-line packages are shipped in one of the carriers shown below. Unless a specific method of shipment is specified by the customer (with possible additional costs), circuits will be shipped in the most practical carrier. Please contact your TI sales representative for the method that will best suit your particular needs.

Dual-in-line (J, JT, N, NT)

- Slide Magazines
- A-Channel Plastic Tubing
- Barnes Carrier (N only)
- Sectioned Cardboard Box
- Individual Plastic Box

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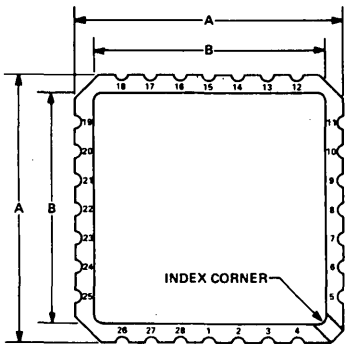
FH and FK ceramic chip carrier packages

Both versions of these hermetically sealed chip carrier packages have ceramic bases. The FH package has a single-layer base with a ceramic lid and glass seal. The FK package has a three-layer base with a metal lid and braze seal.

The packages are intended for surface mounting on solder lands on 1,27 (0.050-inch) centers. Terminals require no additional cleaning or processing when used in soldered assembly.

FH and FK packages are identical to the FC and FD packages, respectively. The new designations are used to indicate devices whose terminal assignments conform to a forthcoming JEDEC Standard.

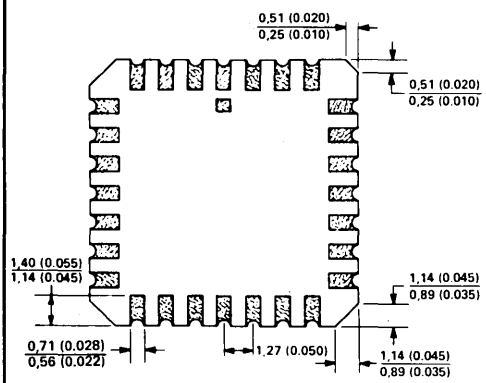
FH AND FK CERAMIC CHIP CARRIER PACKAGES
(28-terminal package shown)

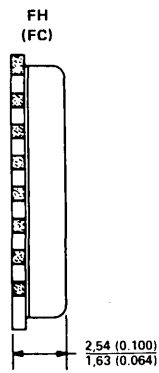


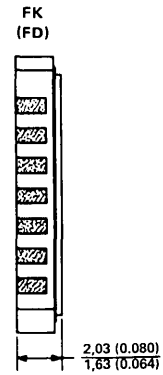
CERAMIC CHIP CARRIERS

JEDEC OUTLINE DESIGNATION*	NO. OF TERMINALS	A MIN	A MAX	B MIN	B MAX
MS004CB	20	8,69 (0.342)	9,09 (0.358)	7,80 (0.307)	9,09 (0.358)
MS004CC	28	11,23 (0.442)	11,63 (0.458)	10,31 (0.406)	11,63 (0.458)
MS004CD	44	16,26 (0.640)	16,76 (0.660)	12,58 (0.495)	14,22 (0.560)
MS004CE	52	18,78 (0.739)	19,32 (0.761)	12,58 (0.495)	14,22 (0.560)
MS004CF	68	23,83 (0.938)	24,43 (0.962)	12,6 (0.495)	21,8 (0.862)
MS004CG	84	28,83 (1.135)	29,59 (1.165)	12,6 (0.495)	27,0 (1.065)

*All dimensions and notes for the specified JEDEC outline apply.







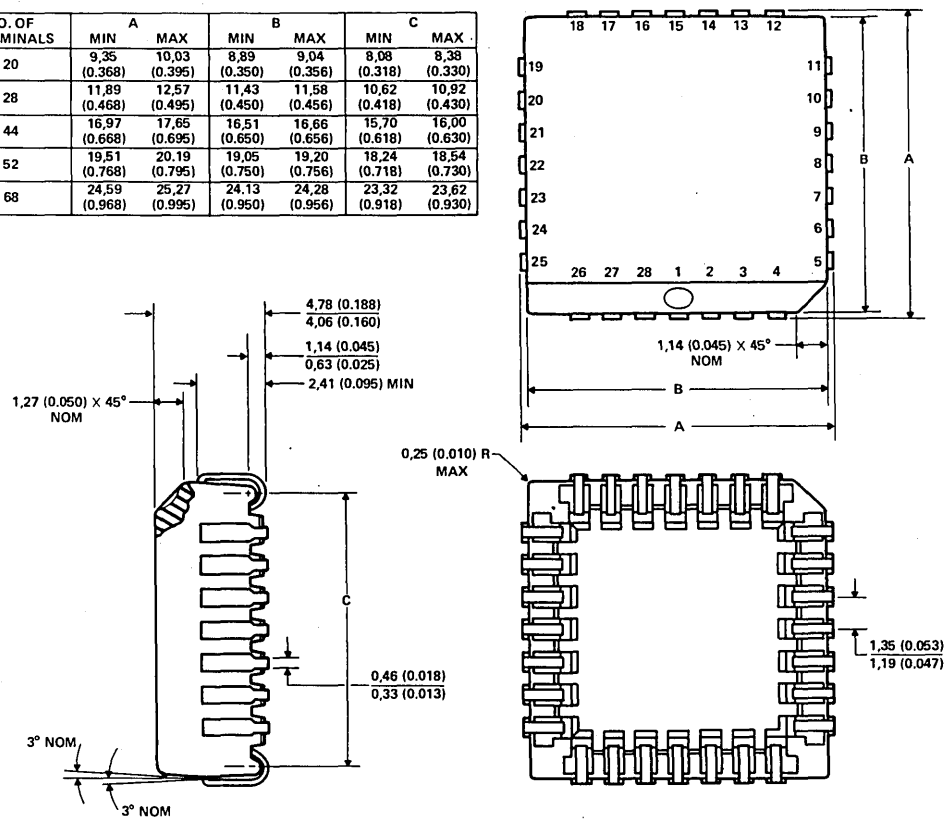
ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

FN plastic chip carrier package

Each of these chip carrier packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The packages are intended for surface mounting on solder lands on 1,27-mm (0.050-inch) centers. Leads require no additional cleaning or processing when used in soldered assembly.

FN PLASTIC CHIP CARRIER PACKAGE
(28-terminal package shown)

NO. OF TERMINALS	A MIN	A MAX	B MIN	B MAX	C MIN	C MAX
20	9,35 (0.368)	10,03 (0.395)	8,89 (0.350)	9,04 (0.356)	8,08 (0.318)	8,38 (0.330)
28	11,89 (0.468)	12,57 (0.495)	11,43 (0.450)	11,58 (0.456)	10,62 (0.418)	10,92 (0.430)
44	16,97 (0.668)	17,65 (0.695)	16,51 (0.650)	16,66 (0.656)	15,70 (0.618)	16,00 (0.630)
52	19,51 (0.768)	20.19 (0.795)	19,05 (0.750)	19,20 (0.756)	18,24 (0.718)	18,54 (0.730)
68	24,59 (0.968)	25,27 (0.995)	24.13 (0.950)	24,28 (0.956)	23,32 (0.918)	23,62 (0.930)



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

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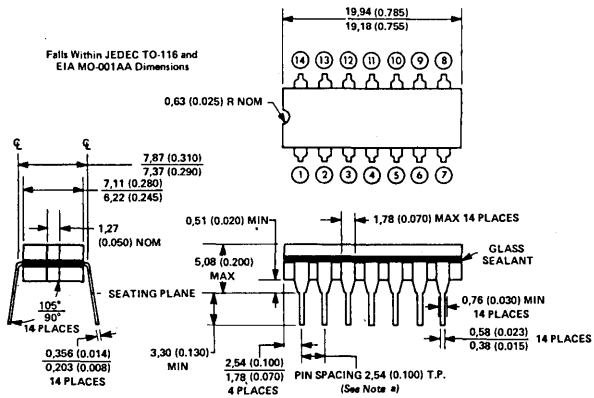
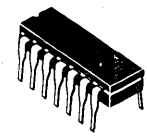
J ceramic packages (including JT packages)

Each of these hermetically sealed dual-in-line packages consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. Once the leads are compressed and inserted sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For the 14-, 16-, and 20-pin packages, the letter J is used by itself since these packages are available only in the 7,62 (0.300) row spacing.

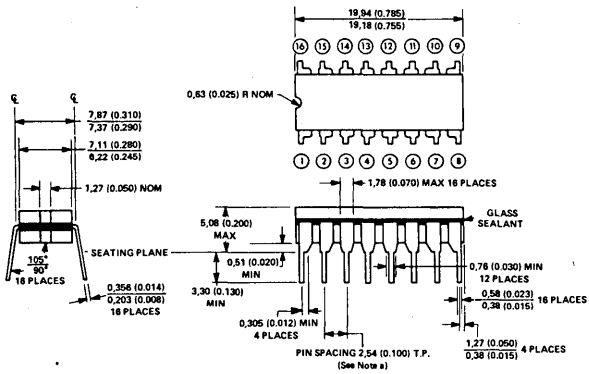
14-PIN J CERAMIC

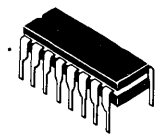




ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

16-PIN J CERAMIC





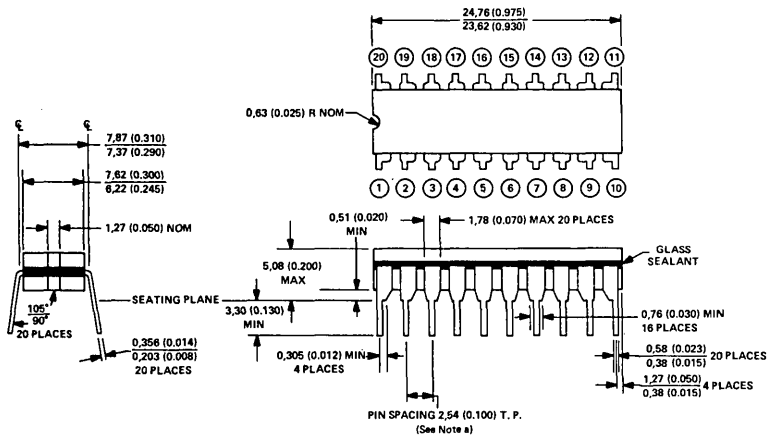
ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

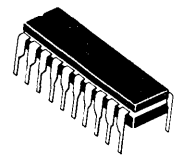
NOTE: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

5

J ceramic dual-in-line packages (continued)

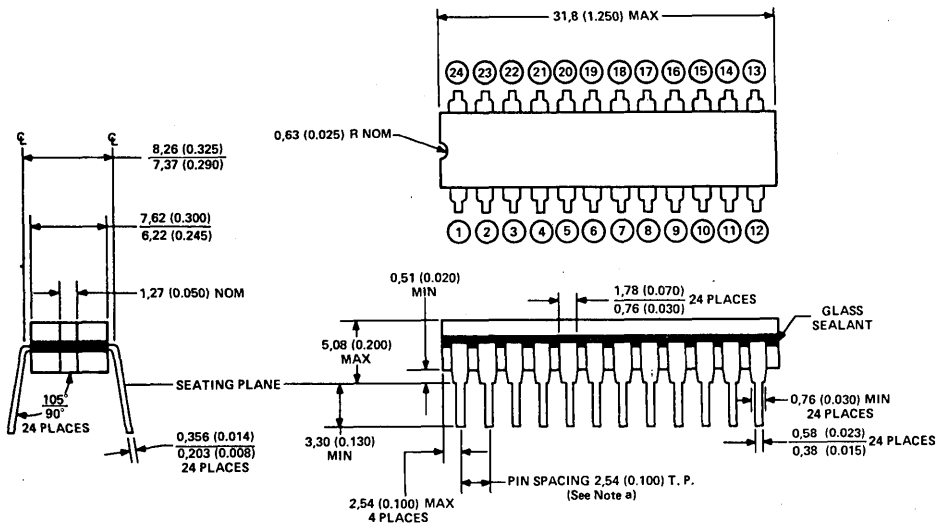
20-PIN J CERAMIC





ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

24-PIN JT CERAMIC



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

NOTE: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

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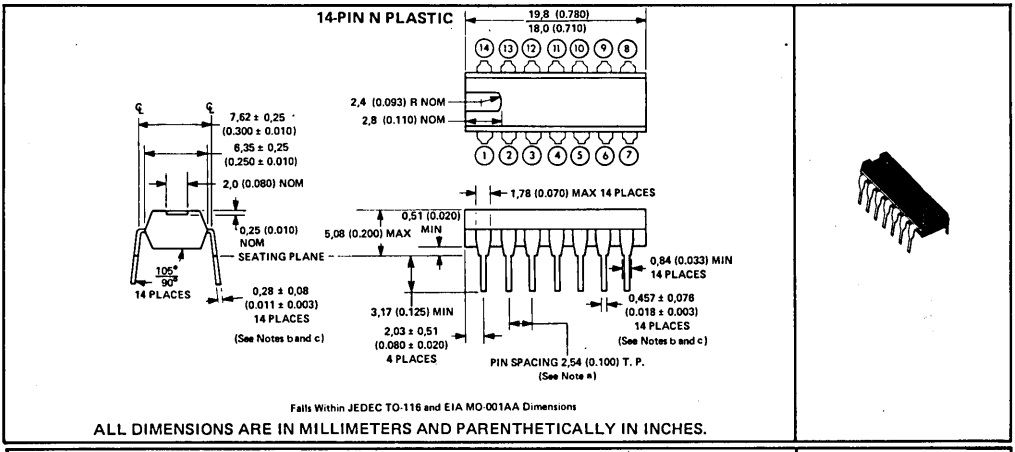
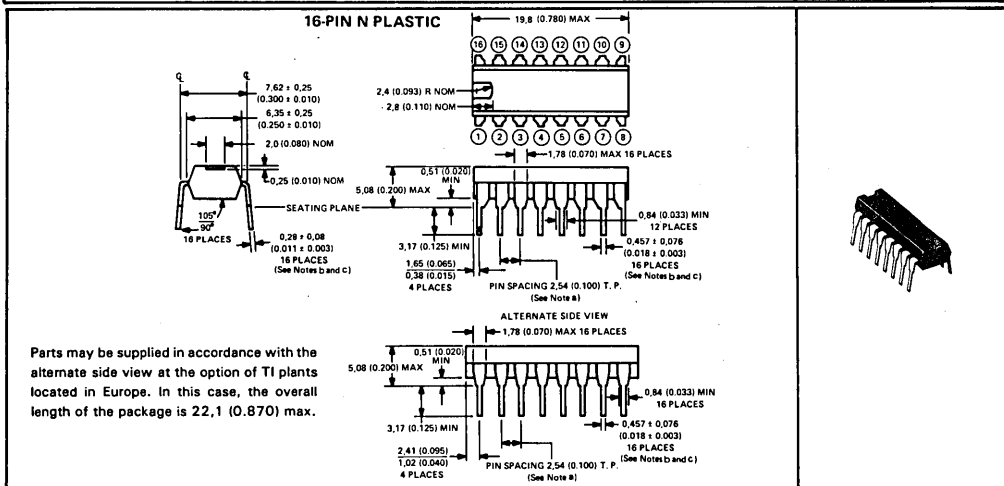
N plastic packages (including NT package)

Each of these dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within an electrically conductive plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For the 14-, 16-, 20-, and 28-pin packages, the letter N is used by itself since these packages are available in only one row-spacing width — 7,62 (0.300) for the 14-, 16-, 18-, and 20-pin packages and 15,24 (0.600) for the 28-pin package.

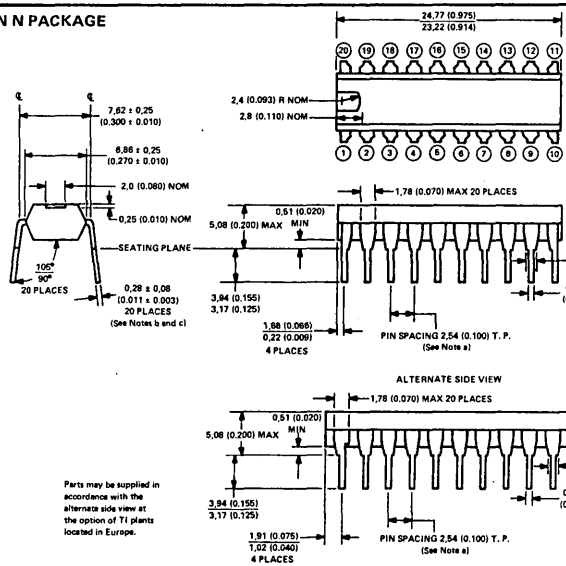


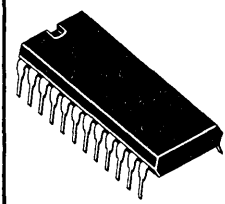


NOTES: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
b. This dimension does not apply for solder-dipped leads.
c. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N plastic dual-in-line packages (continued)

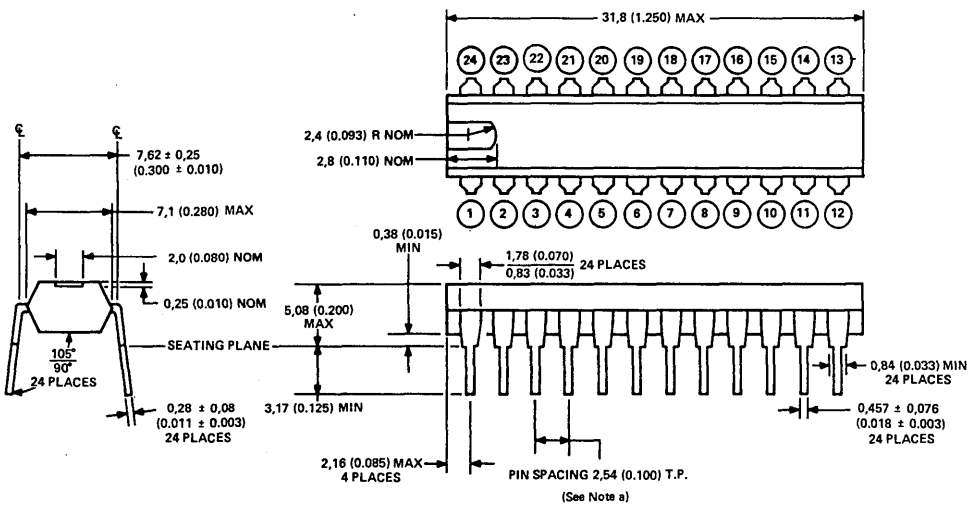
20-PIN N PACKAGE





ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

24-PIN NT PLASTIC



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

NOTES: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
b. This dimension does not apply for solder-dipped leads.
c. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

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IC Sockets

6

IC SOCKETS

Texas Instruments lines of off-the-shelf interconnection products are designed specifically to meet the performance needs of volume commercial applications. They provide both the economy of a standard product line and performance features developed after many year's experience with custom designs. Foremost among these is our ability to selectively bond a wrought gold stripe at the contact point. No waste. Reduced cost. Reliable contacts.

Wrought Gold Contact

Plate a contact with gold and you get a better contact. More reliable, longer lasting. Increase the gold, you improve the contact. But gold is precious, so improved performance has to be costly – right? Wrong. Because now you can get the gold only where it is needed – at the point of contact.

How? With selective metallurgical bonding; a gold stripe inlay. Not porous plating, but durable wrought gold bonded to the contact by the same technology used to produce clad coins and thermostat metals.

Texas Instruments, Attleboro, Massachusetts, is the world's largest producer of these multimetal systems. We also know our way around electronics. The result? A full line of reliable, low cost, interconnection systems featuring an extra measure of gold where it's needed. Premium performance at no premium in price.

IC Sockets

Texas Instruments family of IC sockets includes every type and size in common use today, and as wide a choice of contact materials as you'll find anywhere. Choose from open or closed entry *wire-wrapped*† sockets, standard or low profile solder tail sockets, cable plugs, and component platforms. Sizes from 8 to 40 pins.

Additional information including pricing and delivery quotations may be obtained from your nearest TI Distributor, TI Representative, or:

Texas Instruments Incorporated
Connector Systems Department
MS 14-3
Attleboro, Massachusetts 02703
Telephone: (617) 699-3800
TELEX: ABORA927708

†Registered trademark of Gardner-Denver

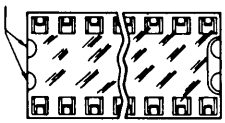
LOW PROFILE SOCKETS

SOLDER TAIL

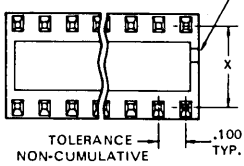
C-93 SERIES GOLD-CLAD CONTACTS

- **Universal mounting and packaging**
- **Anti-wicking wafer**
- **Stand-off tabs on base for solder flush**
- **Redundant contact points for low contact resistance, high reliability and repetitive insertion**
- **Closed entry construction**

SOLDER STANDOFF



IDENTIFICATION NOTCH FOR PIN NO. 1

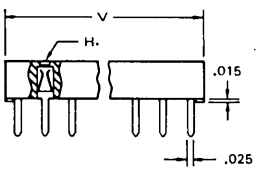


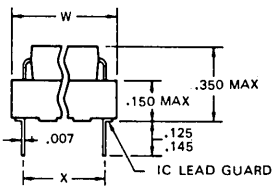
MATERIAL:

A. Body-glass filled nylon (GFN)
B. Contact-copper nickel alloy
C. Finish-see part number schedule

NOTES:

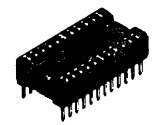
A. Sockets meet requirements of Texas Instruments test specification TS-0005 and test report TR-0003
B. Operating temperature –65°C to ±150°C
C. Contacts have redundant spring elements
D. Accommodates standard IC leads up to .024" square, rectangular, or .024" diameter
E. Contact is designed and oriented in the plastic body to generate maximum possible contact pressure
F. Socket is designed to achieve maximum density on boards
G. Sockets may be mounted end to end on .100" centers continuous line or on .400" centers row to row
H. Socket to be designed to prevent IC leads from contacting P.C. board
I. Closed entry feature provided to facilitate automatic IC insertion and protects the IC leads against damage





	8 Pin	14 Pin	16 Pin	18 Pin	20 Pin	22 Pin	24 Pin	28 Pin	40 Pin
Dimension X ±.005	.300	.300	.300	.300	.300	.400	.600	.600	.600
Dimension V ±.010	.400	.700	.800	.900	1.000	1.100	1.200	1.400	2.000
Dimension W (max)	.400	.400	.400	.400	.400	.500	.700	.700	.700

PART NUMBER SCHEDULE



BLACK BODY

Pins	
8	C9308-02
14	C9314-02
16	C9316-02
18	C9318-02
20	C9320-02
22	C9322-02
24	C9324-02
28	C9328-02
40	C9340-02

CONTACT FINISH
50 microinch minimum gold strip inlay

6

STANDARD PROFILE SOCKET

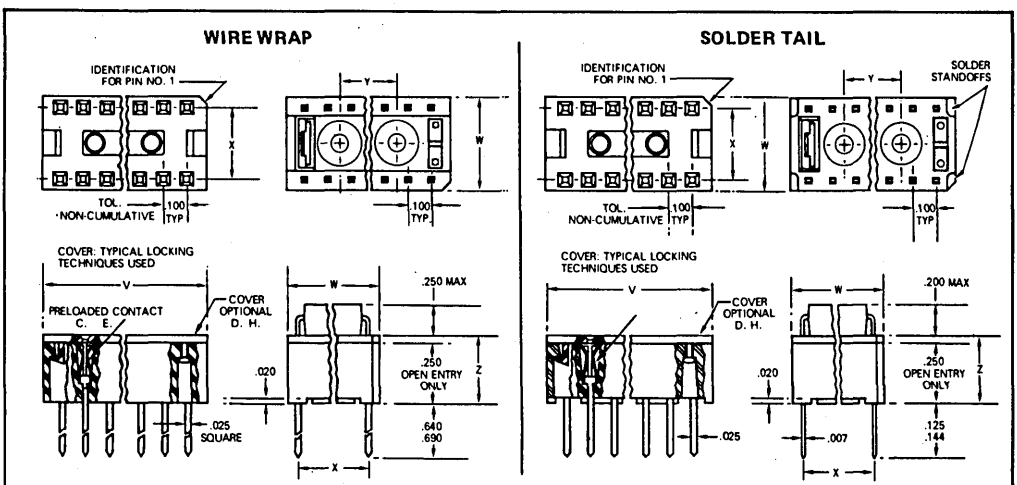
SOLDER TAIL

C-82 SERIES PLATED CONTACTS • C-92 SERIES GOLD CLAD CONTACTS

WIRE WRAP

C-81 SERIES PLATED CONTACTS • C-91 SERIES GOLD CLAD CONTACTS

- Designed for low cost, reliable, high density production packaging
- Universal mounting and packaging capabilities
- 8 to 40 pin lead configurations
- Contacts accommodate .015" through .024" rectangular or round dual-in-line leads
- Wire wrap posts held to true position of .015" providing a true position of .020" on boards for efficient automatic wire wrapping



MATERIAL:

A. Body-glass filled nylon (GFN)
B. Contact-phosphor bronze per QQ-B-750 (C-81) copper nickel alloy (C-91)
C. Finish-see part number schedule

NOTES:

A. Sockets meet requirements of Texas Instruments test specification TS-0003 and test report TR-0001
B. Contacts are replaceable
C. Contacts have redundant spring elements
D. Cover is removeable
E. Contact is designed and oriented in the plastic body to generate maximum possible contact pressure
F. Operating temperature –65°C to +150°C
G. Sockets are designed to achieve maximum density on boards and may be mounted .400" row to row centers
H. Closed entry cover is provided to facilitate automatic insertion and protect IC leads against damage
I. Accommodates standard IC leads up to .024" square, rectangular or .024" dia.
J. Contact retention – 7 lbs. min.
K. Sockets are capable of being automatically or semiautomatically wire wrapped

	8 Pin	14 Pin	16 Pin	18 Pin	20 Pin	24 Pin	28 Pin	36 Pin	40 Pin
Dimension V ±0.10	.465	.765	.865	.965	1.065	1.280	1.480	1.845	2.045
Dimension W (max)	.400	.400	.400	.400	.400	.700	.700	.700	.700
Dimension X ±.005	.300	.300	.300	.300	.300	.600	.600	.600	.600
Dimension Y ±0.10	NA	.400	.400	.400	.400	.500	.500	.800	1.000
Dimension Z ±.005	.280	.280	.280	.280	.280	.280	.280	.325	.325

WIRE WRAP

		OPEN ENTRY	CLOSED ENTRY
PART NUMBER SCHEDULE			
Contact Finish	**Pins**	**Black Body**	**Black Cover**
Series **C-81** 200-400 microinch min tin per MIL-T-10727	8	C810854	C810804
	14	C811454	C811404
	16	C811654	C811604
	18	C811854	C811804
	20	C812054	C812004
	24	C812454	C812404
	28	C812854	C812804
	36		C813604
	40		C814004
Series **C-91** 50 microinch min gold stripe inlay	8	C910850	C910800
	14	C911450	C911400
	16	C911650	C911600
	18	C911850	C911800
	20	C912050	C912000
	24	C912450	C912400
	28	C912850	C912800
	36		C913600
	40		C914000

SOLDER TAIL

		OPEN ENTRY	CLOSED ENTRY
PART NUMBER SCHEDULE			
Contact Finish	**Pins**	**Black Body**	**Black Cover**
Series **C-82** 30 microinch min gold per MIL-G-45204 over 50 microinch min nickel per QQ-N-290	8	C820850	C820800
	14	C821450	C821400
	16	C821650	C821600
	18	C821850	C821800
	24	C822450	C822400
	28	C822850	C822800
	36		C823600
	40		C824000
Series **C-82** 50 microinch min gold per MIL-G-45204 over 100 microinch min nickel per QQ-N-290	8	C820852	C820802
	14	C821452	C821402
	16	C821652	C821602
	18	C821852	C821802
	24	C822452	C822402
	28	C822852	C822802
	36		C823602
	40		C824002
Series **C-82** 200-400 microinch min tin per MIL-T-10727	8	C820854	C820804
	14	C821454	C821404
	16	C821654	C821604
	18	C821854	C821804
	24	C822454	C822404
	28	C822854	C822804
	36		C823604
	40		C824004
Series **C-92** 100-microinch min gold stripe inlay	8	C920850	C920800
	14	C921450	C921400
	16	C921650	C921600
	18	C921850	C921800
	24	C922450	C922400
	28	C922850	C922800
	36		C923600
	40		C924000

SINGLE BEAM SOCKETS

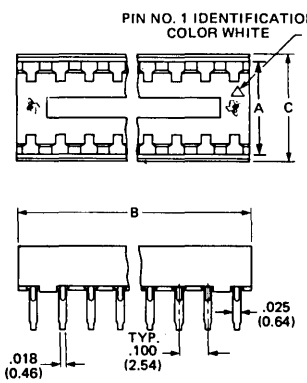
LOW PROFILE/HIGH RETENTION

C87 SERIES BERYLLIUM COPPER CONTACTS

The C87 socket utilizes a beryllium copper contact spring with a 200μ inch minimum tin alloy finish in the contact area. This contact system has been recognized as the standard high performance combination. The system maintains the highest withdrawal and normal forces, along with the ability to retain these properties after cycling.

C88 SERIES PHOSPHOR BRONZE CONTACTS

The C88 socket utilizes a specially processed high-strength copper alloy spring with a 200μ inch minimum tin alloy finish in the contact area. This uniquely engineered contact system has been designed to achieve the performance characteristics that normally require a beryllium copper spring. The device, available at a significantly lower cost than the beryllium copper version, offers the advantage of a substantial cost reduction without sacrificing critical performance requirements.



MATERIAL:

A. Body — Glass reinforced polyester UL rating 94V-0.

*B. Contacts — C87 Series, beryllium copper — C88 Series, phosphor bronze.

C. Contact finish — tin plate: 200μ micro inch min. thick in contact area.

NOTES:

A. Operating temperature: -40°C to +105°C

B. Contact rating: 1 amp

C. Contact capacitance: 2 picofarads max.

D. Contact resistance: 20 milliohms max.

E. Dielectric withstanding voltage: 1000 V.A.C. min.

F. Insulation resistance: 100,000 megohms min.

G. Insertion force — 16 position "blunt IC" (.010 lead): .5#/lead nominal

H. Withdrawal force (.008 test blade)
C87 Series
Initial: 155 gm nominal
After probing with a .014 blade: 98 gm nominal
After probing with a .025 blade: 87 gm nominal
C88 Series
Initial: 112 gm nominal
After probing 2 times with .014 blade: 82 gm nominal
After probing 2 times with .025 blade: 29 gm nominal

I. Normal force (.010 deflection): 250 gm min.

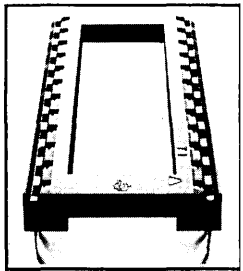
J. Polarization identification: a white circle at the #1 position.

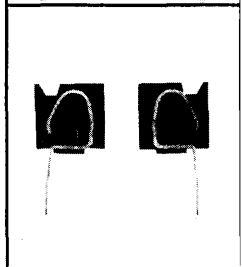
K. Full test reports, #TR 801015 for C87 Series and #TR 810112 for C88 Series, are available from your local sales office.

	8 Pin	14 Pin	16 Pin	18 Pin	20 Pin	22 Pin	24 Pin	28 Pin	40 Pin
Dimension A	(7,62) .300	(7,62) .300	(7,62) .300	(7,62) .300	(7,62) .300	(10,16) .400	(15,24) .600	(15,24) .600	(15,24) .600
Dimension B	(10,16) .400	(17,78) .700	(20,32) .800	(22,86) .900	(25,40) 1.000	(27,90) 1.100	(30,48) 1.200	(35,36) 1.400	(50,80) 2.000
Dimension C	(9,40) .370	(9,40) .370	(9,40) .370	(9,40) .370	(9,40) .370	(11,94) .470	(17,02) .670	(17,02) .670	(17,02) .670

*Also available: C98-Gold Inlay, C89-Copper Alloy

PART NUMBER SCHEDULE





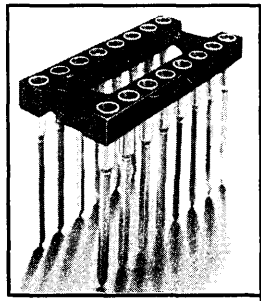
Pins	C87 SERIES	C88 SERIES
8	C8708-01	C8808-01
14	C8714-01	C8814-01
16	C8716-01	C8816-01
18	C8718-01	C8818-01
20	C8720-01	C8820-01
22	C8722-01	C8822-01
24	C8724-01	C8824-01
28	C8728-01	C8828-01
40	C8740-01	C8840-01

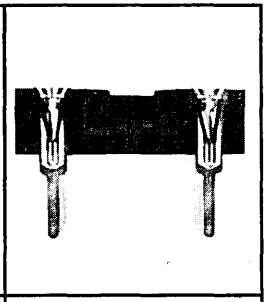
SCREW MACHINE SOCKETS

LOW PROFILE

C71 SERIES WIRE WRAP • C72 SERIES SOLDER TAIL

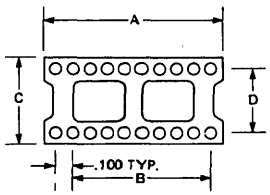
- **Gold contacts with gold sleeve or tin sleeve**

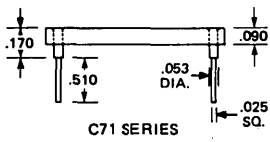




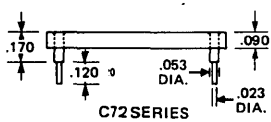
PART NUMBER SCHEDULE

Pins	GOLD SLEEVES C71 Wire Wrap	GOLD SLEEVES C72 Solder Tail
6	C7106-03*	C7206-09*
8	C7108-03	C7208-09
14	C7114-03	C7214-09
16	C7116-03	C7216-09
18	C7118-03	C7218-09
20	C7120-03	C7220-09
22	C7122-03	C7222-09
24	C7124-03	C7224-09
28	C7128-03	C7228-09
40	C7140-03	C7240-09
64	C7164-03*	C7264-09*
	TIN SLEEVES	
6	C7106-53*	C7206-59*
8	C7108-53	C7208-59
14	C7114-53	C7214-59
16	C7116-53	C7216-59
18	C7118-53	C7218-59
20	C7120-53	C7220-59
22	C7122-53	C7222-59
24	C7124-53	C7224-59
28	C7128-53	C7228-59
40	C7140-53	C7240-59
64	C7164-53*	C7264-59*





C71 SERIES



C72 SERIES

MATERIAL:

A. Body — Thermoplastic, meeting UL specification 94-V-O

B. Contact — Beryllium copper QQ-C-530, finish — gold over nickel per mil-G-45204

C. Sleeve — Brass QQ-B-626, finish — gold over nickel per mil-G-45204 or tin over nickel per mil-T-10727

NOTES:

A. Open body construction and high standoffs provide improved cleaning and heat dissipation

B. Accept standard I.C. leads .010± .003 x .018± .003 or .010 to .022 dia.

C. Accept I.C. lead lengths from .090 to .155

D. Operating temperatures:
Gold sleeve -65°C to 125°C
Tin sleeve -40°C to 100°C

E. Performance — meets req. of T.I. test spec. T.S. 0008 as shown in test report T.R. 1021.

	6 Pin	8 Pin	14 Pin	16 Pin	18 Pin	20 Pin	22 Pin	24 Pin	28 Pin	36 Pin	40 Pin	64 Pin
Dimension A max.	.300	.400	.700	.800	.900	1.000	1.100	1.200	1.400	1.800	2.000	3.200
Dimension B ±.005	.200	.300	.600	.700	.800	.900	1.000	1.100	1.300	1.700	1.900	3.100
Dimension C max.	.400	.400	.400	.400	.400	.400	.500	.700	.700	.700	.700	1.000
Dimension D ±.005	.300	.300	.300	.300	.300	.300	.400	.600	.600	.600	.600	.900

Note: Contacts for one- and two-level wire wrapping are also available. Contact the factory for details.

*Minimum order requirements on these parts. Alternate insulator materials may be used.

6

SPECIAL SOCKETS

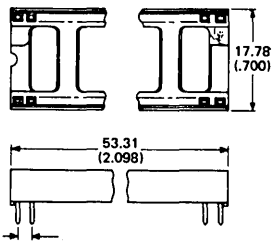
SLIM PACKAGE

C8424-03 • C9324-03

.300 row to row spacing on the low profile edgegrip

42 POSITION

C4742-11



MATERIAL:

A. Body: 94V-0 glass filled polyester

B. Contact: Copper alloy

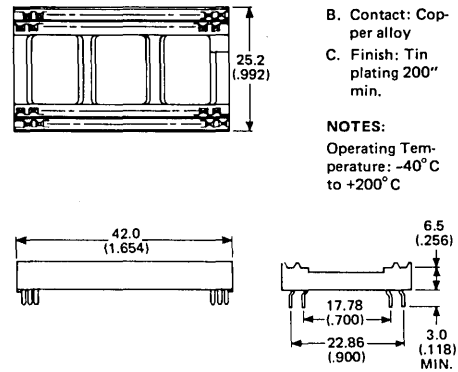
C. Finish: Tin plating: 120" min.

NOTES:

A. Operating temperature: -40°C to +100°C

QUAD PACKAGE

C4W64-11 SERIES 64 STAGGERED PINS



MATERIAL:

A. Body: Ryton R-8

B. Contact: Copper alloy

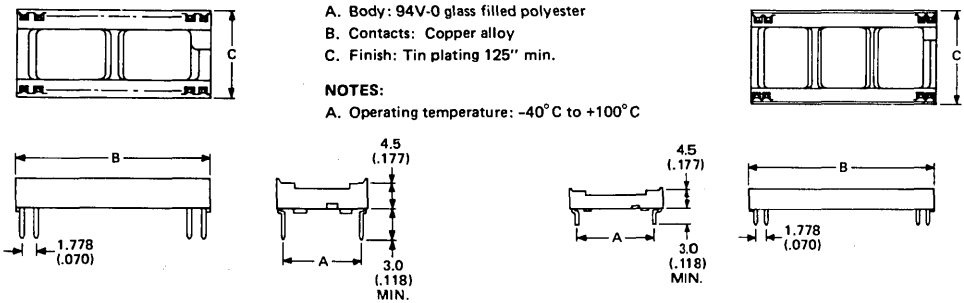
C. Finish: Tin plating 200" min.

NOTES:

Operating Temperature: -40°C to +200°C

SHRINK PACKAGE

C4S SERIES 28 AND 40 POSITIONS



MATERIALS:

A. Body: 94V-0 glass filled polyester

B. Contacts: Copper alloy

C. Finish: Tin plating 125" min.

NOTES:

A. Operating temperature: -40°C to +100°C

Part No.	Pos.	A	B	C
C4S28-02	28	10.16 (.400)	25.0 (.984)	13.0 (.512)
C4S40-02	40	15.24 (.600)	35.7 (1.406)	18.0 (.709)

6

TEXAS INSTRUMENTS